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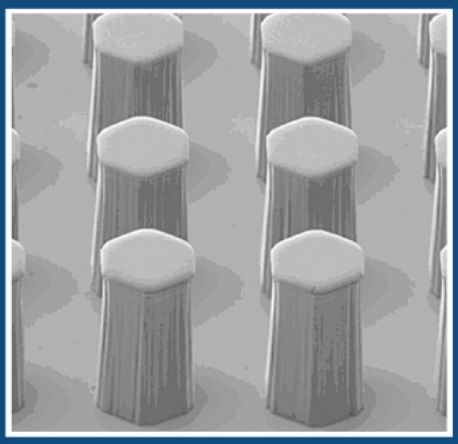

# Electromigration in thin films and electronic devices

## Materials and reliability

Edited by Choong-Un Kim

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# Electromigration in thin films and electronic devices

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# Electromigration in thin films and electronic devices

## Materials and reliability

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# 1

# Modeling of electromigration phenomena

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**Abstract**: From early Black's law to modern technology computer-aided design (TCAD) solutions, this chapter highlights the different strategies of electromigration modeling. Firstly, vacancy transport equations are discussed and applications to interconnect failure mode are described. Then, the simulation of void shape evolution during electromigration is presented and various numerical methods are compared and illustrated.

**Key words**: electromigration modeling, Black's law, void shape evolution.

## 1.1 Introduction

Electromigration is a mass transport process operating in metal films stressed under electrical current. The atomic transport is a result of momentum transfer between conduction electrons and lattice atoms as a result of collisions in the ohmic conduction regime. Over time, temperature and current stress, macroscopic voids may develop and lead to an increase in line resistance or even a complete open circuit.

Electromigration presents a strong challenge to the development of advanced interconnects for integrated circuits (ICs). Not only must new materials and architectures be developed to realize high performance ICs, but also accurate models of electromigration degradation are needed to predict the lifetime of chips and establish safe design rules. Empirical one-dimensional models are now not sufficient to optimize the design of advanced technologies and the use of numerical software to model electromigration has become mandatory. The electromigration phenomenon is also challenging to model because it involves several driving forces and coupled equations as well as several diffusion paths. The diversity of the relevant physical phenomena, and the eventual different time/space scale involved, increases the complexity of mathematical models. However, with the development of efficient computational tools, numerical modeling with a multiphysics approach is now generalized: it is possible to investigate failure mechanisms in detail and also to understand the limitations of earlier empirical models. It is therefore a powerful tool to study the effect of several parameters such as line geometry, microstructure, and statistical distribution of grain size. In the 1960s, soon after the development of IC chips, the electromigration



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phenomenon was observed in aluminum conductor lines[1,2] and electron wind force was identified to be the driving force responsible for mass transport. Such a formulation was relevant to describe most of the physical failure observations. In the late 1960s, J. R. Black investigated electromigration for an aluminum metallization system.[3,4,5] He expressed the mean time to failure (MTF) of a metal line stressed by a current density $j$ by:

$$MTF = A\frac{wt}{j^2}\exp\left(\frac{E_a}{kT}\right) \quad [1.1]$$

where $A$ is a constant which depends on the technology feature, $w$ and $t$ are, respectively, the width and thickness of the conductor, $E_a$ is the activation energy, $k$ is the Boltzman's constant and $T$ is the temperature. In practice, equation [1.1] is unable to reproduce all experimental observations. In particular, the value of the current density exponent is preferentially expressed by $n$ which needs to be adjusted to fit experimental observations. The $n$ exponent is related to the failure mechanisms involved. Under high current density (>10 MA cm$^{-2}$), typical for wafer level tests, the value of $n$ is reported to be higher than 2, whereas for lower stress current densities, typical for package level tests, most of the $n$ values reported, range from 1 to 2. In the first case, joule heating induces significant temperature gradients, therefore other driving forces need to be considered; this point is developed later.

Although Black's equation is widely accepted by industry as a standard, a reliability engineer still faces the practical issue of extrapolating lifetime from accelerated tests to operating conditions since large variations in current density exponents are reported in the literature. Then, the accuracy of lifetime prediction with such apparent variations is questionable.[6] Among all the possible sources of apparent variation of $n$, we will discuss the effect of temperature gradient, the Blech effect, as well as the competing effects of void nucleation and void growth. Lloyd proposed an analytical formalism to describe the competition of nucleation and growth processes, involving specific kinetic regimes, i.e. specific current density dependencies:

$$MTF = \left(\frac{AT}{j} + \frac{B(T)}{j^2}\right)\exp\left(\frac{E_a}{kT}\right) \quad [1.2]$$

where $A$ is a constant and $B(T)$ a temperature function which is failure mode dependent.[7] In the same way, the activation energy for nucleation and growth need to be distinguished. This expression is validated by measurement: an exponent $n$ close to one means that lifetime is limited by void growth, as shown in Cu metallization, whereas an exponent close to two means a void nucleation limited lifetime,[8,9] typical aluminum metallization behavior. Interestingly, Basaran *et al.*[10] developed a model of damage evolu-

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tion based on thermodynamics, statistical mechanics, and continuum damage mechanics, which agreed with Black's law. In this model, the MTF is expressed by the inverse power of two of the current density. Recently, Montemayor-Aldrete *et al.*[11] enhanced the previous approach; they develop a new theoretical scheme within nonequilibrium statistical physics that takes into account the aging process occurring in a dissipative system. An agreement between their model and measured resistance change was found to be a function of time and stress conditions. However a more accurate model is necessary to extrapolate lifetime from accelerated stress conditions to operating conditions.

In the following section, several one-dimensional comprehensive mass transport models are described; their limitations and strengths are highlighted.

## 1.2 Analytical methods

### 1.2.1 Mass transport equation

Metal atoms migrate via a vacancy exchange mechanism. Thus, the atomic flux is the opposite of vacancies flux, and, thus, under an applied electrical field $E$, the fluxes are expressed as follow:[12]

$$J_{\mathrm{v}} = C_{\mathrm{v}} \frac{e|Z^*|D_{\mathrm{v}}}{kT} E = -C_{\mathrm{a}} \frac{e|Z^*|D_{\mathrm{a}}}{kT} E = -J_{\mathrm{a}} \qquad [1.3]$$

where $C$ is the concentration, $D$ the diffusivity, $kT$ the thermal energy, $Z^*$ the effective charge number and $e$ the elementary charge. The subscripts $v$ and $a$ denote respectively the vacancy and atomic species.

In copper-based interconnects of recent integrated circuits; the double damascene process is used, as presented in the Fig. 1.1. After etching trenches in the interlevel dielectric, a thin layer of TaNTa is sputter deposited with a thin copper seed layer. Then the trench is filled with Cu electroplating. The excess Cu is removed by chemical mechanical polishing (CMP). A thin SiN layer is deposited to isolate and encapsulate the copper line. In order to simplify this complex system where several diffusion paths are involved, a one-dimensional effective diffusivity approach is chosen.

Assuming a copper line of length $L$, width $w$ and height $h$, with columnar grain size $d$, the effective diffusivity is expressed by the contribution of the different diffusion paths:

$$D_{\mathrm{eff}} = D_{\mathrm{lattice}} + \delta_{\mathrm{gb}} \frac{w-d}{wd} D_{\mathrm{gb}} + 2\delta_{\mathrm{i}} \frac{w+h}{wh} D_{\mathrm{i}} \qquad [1.4]$$

where $\delta_{\mathrm{gb}}$ and $\delta_{\mathrm{i}}$ are, respectively, the widths of grain boundary and interface. $D_{\mathrm{lattice}}$, $D_{\mathrm{gb}}$ and $D_{\mathrm{i}}$ are, respectively, diffusivity of lattice, grain boundary and

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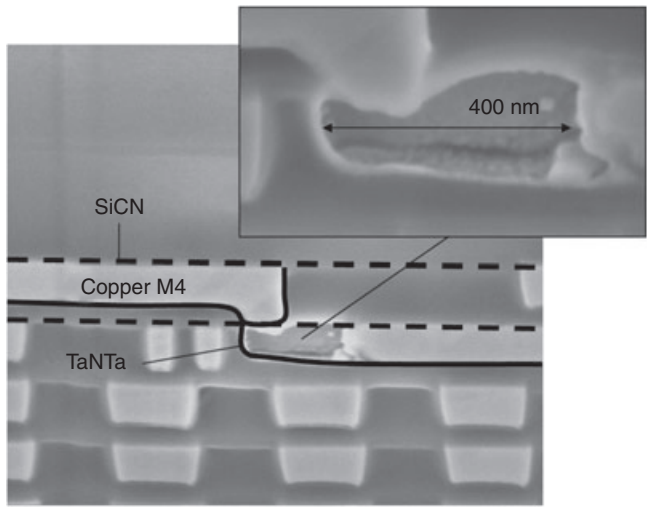


*1.1* Cross-section of void in via 3 metal 3 interconnect. Refractory barrier layer is TaNTa. A thin silicon nitride layer is deposited to isolate and encapsulate the copper line. Technology node is 40 nm and current stress is 5 MA $cm^{-2}$ at 350 °C.

interface. The diffusion characteristics of the interface Cu/SiN and Cu/TaNTa are different; this point will be developed in the next part. For clarity, $D_{\text{eff}}$ is now simply denoted as $D$.

The next vacancy flux along the line length in the $x$ direction is composed of Fickian diffusion term and the electromigration driving force term:

$$J_{\text{v}} = D_{\text{v}}\left(\frac{e|Z^*|C_{\text{v}}}{kT}E - \frac{\partial C_{\text{v}}}{\partial x}\right) \qquad [1.5]$$

The electric field $E$ is replaced by the product of the resistivity $\rho$ times the current density $j$. The mass transport can now be expressed by the following balance equation:

$$\frac{\partial C_{\text{v}}}{\partial t} + \frac{\partial J_{\text{v}}}{\partial x} = R_{\text{v}} \qquad [1.6]$$

where $R$ is a sink/source term which represents the generation and recombination of vacancies. Assuming a constant effective diffusivity, from equations [1.5] and [1.6] it follows that a generic one-dimensional transport equation may be expressed by:

$$\frac{\partial C_{\text{v}}}{\partial t} + D_{\text{v}}\frac{\partial}{\partial x}\left(\frac{e|Z^*|\rho j}{kT}C_{\text{v}} - \frac{\partial C_{\text{v}}}{\partial x}\right) = R_{\text{v}} \qquad [1.7]$$

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Several solutions of equation [1.7] are now reviewed. The first solution provides for the case where $R_v$ is null. This is the form of the equation that was investigated by Shatzkes and Lloyd[13] and Clement and Lloyd.[14] They investigated the vacancies evolution at the end of a semi-infinite line and in a finite line, respectively. For a semi-infinite line, boundary conditions for the variable $C_v$ are given by $C_v(-\infty, t) = C_{v0}$ and $J_v(0, t) = 0$ which means that the concentration at the boundary $x = -\infty$ remains at its equilibrium value and the flux at location $x = 0$ is blocked. $C_v(x, t)$ solution is given by a Laplace transformation:

$$C_v(0,t) = C_{v0} + C_{v0}\text{erf}\beta + 2C_{v0}\left[\beta^2(1+erf\beta) + \frac{\beta}{\sqrt{\pi}}\exp(-\beta^2)\right] \qquad [1.8]$$

where $\beta = \dfrac{e|Z^*|\rho j}{2kT}\sqrt{D_v t}$. Shatzkes and Lloyd suggested that a critical vacancy concentration $C_{vc}$ was needed to nucleate a void, and thus failure soon followed the nucleation void. Following this statement, equation [1.8] is developed assuming $\beta >> 0$, the critical $C_{vc}$ is reached at time to failure $t_f$:

$$C_{vc}(0,t) = C_{v0}\left(\frac{e|Z^*|\rho j}{kT}\right)^2 D_v t_f \qquad [1.9]$$

By using the Arrhenius temperature dependence of the vacancy diffusivity, the time to failure is expressed by:

$$t_f = \frac{AT^2}{j^2}\exp\left(\frac{E_a}{kT}\right) \qquad [1.10]$$

which is similar in form to Black's semi-empirical model of equation [1.1] except for the term $T^2$. The predicted time to failure is inversely dependent on the square of current density.

Another analytic solution of equation [1.7] with a null sink/source term and a finite line of length $L$ is now presented. The flux is blocked at both ends of line: $J_v(0, t) = J_v(-L, t)$. The solution is now:

$$C_v(x,t) = A_0 C_{v0} - C_{v0}\sum_{n=1}^{\infty} A_n \exp\left(-B_n\frac{D_v t}{L^2} + \alpha\frac{x}{2L}\right) \qquad [1.11]$$

where $\alpha = \dfrac{e|Z^*|\rho j}{kT}L$, $A_0 = \dfrac{\alpha}{1-\exp(\alpha)}\exp\left(\alpha\dfrac{x}{L}\right)$,

$$A_n = \frac{16n\pi\alpha^2\left[1-(-1)^n\exp(\alpha/2)\right]}{\left(\alpha^2+4n^2\pi^2\right)^2}\left[\sin\left(n\pi\frac{x}{L}\right) + \frac{2n\pi}{\alpha}\cos\left(n\pi\frac{x}{L}\right)\right]$$

and $B_n = n^2\pi^2 + \alpha^2/4$

An illustration of the vacancy concentration at $x = 0$ is proposed in Fig. 1.2 showing the case of a semi-infinite and a finite line. In the calculation,

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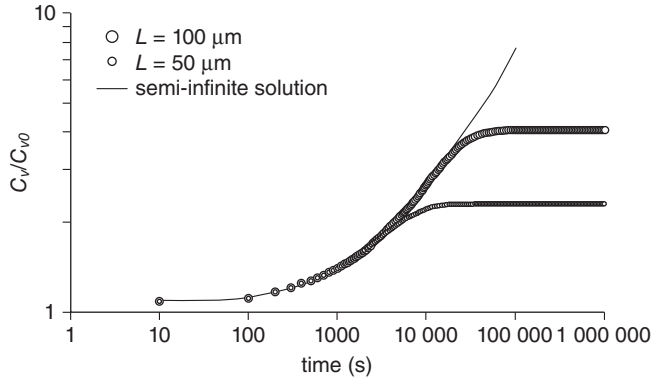
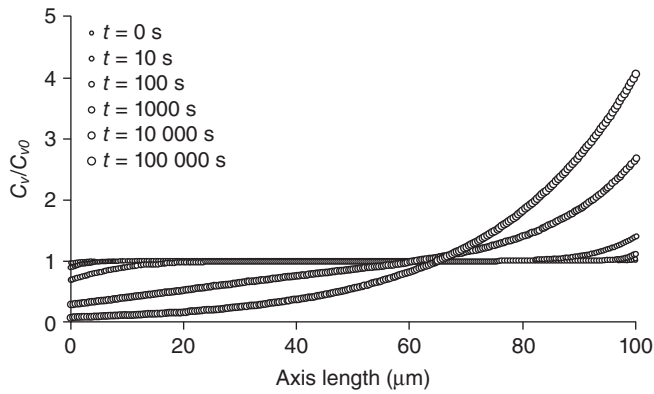



*1.2* Accumulation of vacancy at cathode. The symbols correspond to the results of equation [1.11] for two line lengths. The line represents the semi-infinite solution of equation [1.8].




*1.3* Distribution of relative vacancy concentration along the line length at different diffusion time.

the following set of parameters is chosen: $\rho$, $J$, $T$ and $D_v$ are, respectively, $1.6 \times 10^{-8}$ Ωm, 2 MA cm$^{-2}$, 200 °C and $6 \times 10^{-14}$ m$^2$ s$^{-1}$.

Vacancy concentration is calculated for two different line lengths, the saturation occurs later and at a higher concentration for the larger line than for the smaller one. The semi-infinite solution does not exhibit saturation behavior because the steady state is never reached. Interestingly, the profile of vacancy as a function of diffusion time is not symmetrical with regard to the middle of the line as shown in Fig. 1.3. Indeed the model of transport could be written either in vacancy concentration or atomic concentration because the two species play the same role. The lack of symmetry between accumulation and depletion, respectively, at cathode and anode makes this

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model inadequate. Concerning qualitative results, the lifetime expected with the formalism described in equations [1.9] and [1.10], at a typical stress condition of 200 °C and 2 MA cm$^{-2}$ is smaller than that observed experimentally. Because the time to reach the steady state is too short, as observed by Rosenberg and Ohring,[15] some improvement on this model is needed.

A new term of source/sink, proposed by Kirchheim,[16] is added in the continuity equation.

$$R_{\mathrm{v}} = -\frac{C_{\mathrm{v}} - C_{\mathrm{ve}}}{\tau} \qquad [1.12]$$

where $C_{\mathrm{ve}}$ is the equilibrium concentration of vacancy with the grain and $\tau$ is the average lifetime of vacancy in the grain boundary. Annihilation of grain boundary vacancies occurs if their concentration is higher than equilibrium, and in the opposite case there is generation.

The typical magnitude order of $\tau$ is several milliseconds. Assuming that the equilibrium concentration $C_{\mathrm{ve}}$ remains constant and close to $C_{\mathrm{v0}}$, the numerical solution now becomes symmetrical but saturation is incredibly low and the steady state is reached more quickly. As a consequence, a more accurate expression of $C_{\mathrm{ve}}$ must be found. Considering that the exchange of vacancies with the grain boundary can contribute to change not only the local equilibrium vacancy in the grain but also the local lattice concentration, a constitutive equation of $C_{\mathrm{ve}}$ can be expressed. Two coupled equations need to be solved. Some illustrations of this model were developed by Clement,[17] and the solution highlights a plateau before a saturation regime for $C_{\mathrm{v}}$ in function of time. Moreover when $\tau$ becomes small, $C_{\mathrm{v}}$ is close to $C_{\mathrm{ve}}$.

Another expression of $R_{\mathrm{v}}$ is now developed. In a metallic line embedded in dielectric, the relative atomic concentration of lattice sites $C$ is related to its hydrostatic stress by:

$$\frac{\partial C}{C} = -\frac{\partial \sigma}{B} \qquad [1.13]$$

where $B$ is the effective modulus which depends on the stiffness and thickness of the different materials surrounding the line. The source/sink term can be expressed by:[18]

$$Rv = \frac{\partial C}{\partial t} = -\frac{C}{B}\frac{\partial \sigma}{\partial t} \qquad [1.14]$$

On the other hand, the vacancy concentration is in equilibrium with the mechanical stress:

$$C_{\mathrm{v}} = C_{\mathrm{v0}} \exp\left(\frac{\Omega\sigma}{kT}\right) \qquad [1.15]$$

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Using the expression of $R_v$, the equation [1.7] becomes:

$$\left(\frac{C_v}{C}\frac{\Omega B}{kT}+1\right)\frac{C}{B}\frac{\partial\sigma}{\partial t}=\frac{\partial}{\partial x}\left[\frac{D_v C_v}{kT}\left(\Omega\frac{\partial\sigma}{\partial x}-e|Z^*|\rho j\right)\right] \quad [1.16]$$

Korhonen *et al.*[19] remarked that, in test conditions, the term $(C_v\Omega B)/(CkT) << 1$. Such an approximation, leads to the well known equation:

$$\frac{\partial\sigma}{\partial t}=\frac{\partial}{\partial x}\left[\frac{BD_a\Omega}{kT}\left(\frac{\partial\sigma}{\partial x}-\frac{e|Z^*|\rho j}{\Omega}\right)\right] \quad [1.17]$$

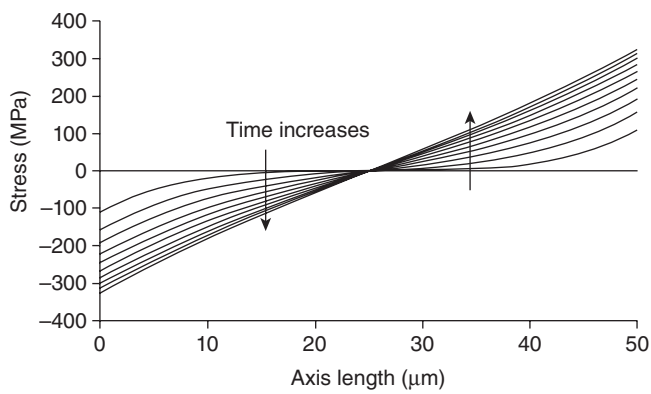
Considering Neumann conditions at both end of the line, $J_v(0, t) = J_v(-L, t) = 0$, an analytic solution is found:[19,20]

$$\sigma=\frac{e|Z^*|\rho j}{\Omega}\left[\frac{1}{2}+\frac{x}{L}-4\sum_{n=0}^{\infty}a_n^{-2}\exp\left(-a_n^2\frac{bt}{L^2}\right)\cos\left(a_n\frac{x}{L}\right)\right] \quad [1.18]$$

where $a_n = (2n + 1)\pi$ and $b=\dfrac{D_a\Omega B}{kT}$

An illustration of equation [1.18] is proposed in Fig. 1.4. For different time steps, the profile of stress along the line is plotted. At the cathode, the accumulation of vacancies leads to tensile stress variation whereas at the anode, the depletion of vacancies leads to compressive stress variation. The stress calculated in equation [1.18] is not representative of the absolute value of the mechanical stress in the line because the mechanical equilibrium is not solved. Thus, it should be taken as the variation of the mechanical stress state from an initial condition.

The equation [1.17] written in stress can also be expressed in vacancy concentration $C_v$:




*1.4* Stress build-up in the line for different time steps $J = 2$ MA cm$^{-2}$.

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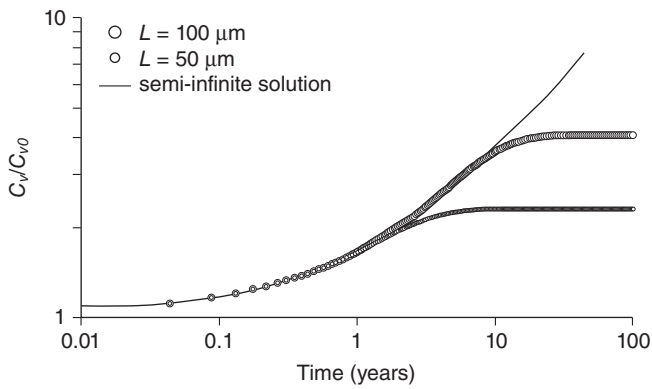
$$\frac{\partial C_v}{\partial t} + \frac{\partial}{\partial x}\left[\frac{BD_a\Omega}{kT}\left(e|Z^*|\rho j C_v - \frac{\partial C_v}{\partial x}\right)\right] = 0 \qquad [1.19]$$

This equation is presented in the same form as equation [1.7] without a sink/source term, for which the term $BD_a\Omega/kT$ is replacing $D_v$. The consequence is a time-scaling change, so that rather than a lifetime in hours obtained previously in equation [1.7] the lifetime is calculated in days in equation [1.19] (Fig. 1.5). As suggested by Clement,[17] diffusion, controlling stress evolution, is a very slow process compared with the build-up of vacancies without considering the role of stress on the recombination/generation of vacancies.

It worth noting that equations [1.17] and [1.19] enable various phenomena not developed here to be explored. The contribution of atomic sinks and reservoirs can be explained with simulation.[21] Moreover, by integrating the atoms drifted into the line, the evolution of void volume as a function of time can be assessed; He *et al.*[22] related electromigration lifetime to the saturation void volume. More recently, the effect of grain size was identified, by Dong *et al.*, as playing a role in the maximal stress achieved at the steady state.[23]

## 1.2.2 Blech effect

Previous models highlight that when considering only the Fickian term of vacancy and the electromigration term, the time scale of transport was not comparable to the one observed in experiments. Assuming a void nucleation limited by critical vacancy concentration, the time to failure calculated




*1.5* Accumulation of vacancies at the cathode. The symbols correspond to the results of equation [1.17] for two line length. The line represents the semi-infinite solution. The solution is identical to the one of Fig. 1.2 but the time is rescaled by several decades.

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with such simple models fails. When mechanical stress is introduced this shortcoming is resolved.

In 1976, Blech[24] and Blech and Herring[25] found that mass transport reached a steady state when the conductor length was smaller than a critical value (~30 μm) for a given stress condition, below this length, no failure occurs. He observed also that there was no mass transport below a threshold current density. Blech suggested that the presence of a 'back flow' of atoms opposite to the electron direction owing to the presence of back stress could explain the steady state regime. If we are considering the flux of a vacancy expressed with the electromigration term, the gradient of mechanical stress is:

$$J_{\mathrm{v}} = \frac{D_{\mathrm{v}}C_{\mathrm{v}}}{kT}\left(e|Z^*|\rho j - \Omega\frac{\partial\sigma}{\partial x}\right) \qquad [1.20]$$

This form is the same as in equation [1.19]. The gradient of mechanical stress, referred to as 'back flow', opposes the electromigration flux and when the two terms are equal, the net flux becomes null and the steady state is reached. This condition is the Blech condition given by:

$$\frac{\partial\sigma}{\partial x} = \frac{e|Z^*|\rho j}{\Omega} \qquad [1.21]$$

Integrating along the line length we find a solution for the stress:

$$\sigma = \sigma_0 + \frac{e|Z^*|\rho j}{\Omega}x$$

where $\sigma_0$ is the stress at $x = 0$. This is a residual stress in the line owing to mismatch of thermal expansion between the line and the surrounding dielectric and process-induced stress.

Assuming a stress yield which corresponds to void nucleation $\sigma_{\mathrm{y}}$ the famous critical product for electromigration failure can be expressed by:

$$(jL)_{\mathrm{c}} = \frac{(\sigma_{\mathrm{y}} - \sigma_0)\Omega}{e|Z^*|\rho} \qquad [1.22]$$

This is also called the Blech product. Typical values for this critical product range from 2500 (copper/low-$k$) to 6000 A cm$^{-1}$ (copper/$SiO_2$).[26] This model perfectly accounts for experimental results where, under certain $j \times L$ stress conditions, electromigration failure does not occur within a reasonable observation time. This situation is currently referred to as 'immortality' versus electromigration. However, it is worth noting that, even if stress build-up is likely to generate back flow until total compensation for electromigration flux, a significant amount of metal is moving in the transitory phase. Therefore, depletion on the cathode side results in a

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resistance change that may or may not reach the failure criteria. The subsequent resistance change $\Delta R/R$ will naturally saturate with time to a certain value, $(\Delta R/R)_{sat}$, as described by Filippi *et al.*[27] who demonstrated that, at saturation, the length of the depleted region that contributes to the resistance increase follows a $j \times L^2$ dependence.

Moreover, for any given depleted copper trench volume, there is a corresponding given strain to accommodate the excess copper volume increase. In the steady-state regime, the corresponding mechanical stress built-up is function of void volume and initial stress as:

$$V = \frac{\sigma_0 L_c}{B} + \frac{\Delta\sigma L_c}{2B} \qquad [1.23]$$

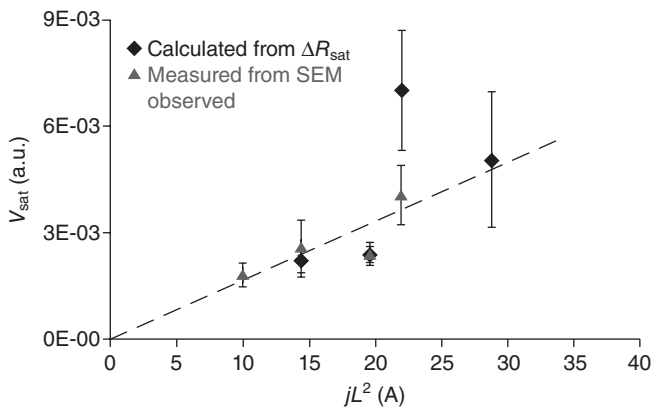
Considering the steady state condition, where back flow totally compensates for electromigration, gives:

$$V = \frac{\sigma_0 L_c}{B} + \frac{j\rho e Z^* L_c^2}{2\Omega B} \qquad [1.24]$$

This model illustrates that void size, eventually producing an electrical failure, is a function of $j \times L^2$. In other words, under a given $j \times L^2$ threshold, void size is too small to induce an electrical failure. This model fits experimental observations from Lamontagne *et al.*[28] (Fig. 1.6).

## 1.2.3 Consequences of the lifetime prediction method

As reported in the previous section, the Blech effect is likely to counteract electromigration so that mass transport is reduced to a certain extent or




*1.6* Evolution of void size measured from SEM observation and void size calculated from measured resistance increase.

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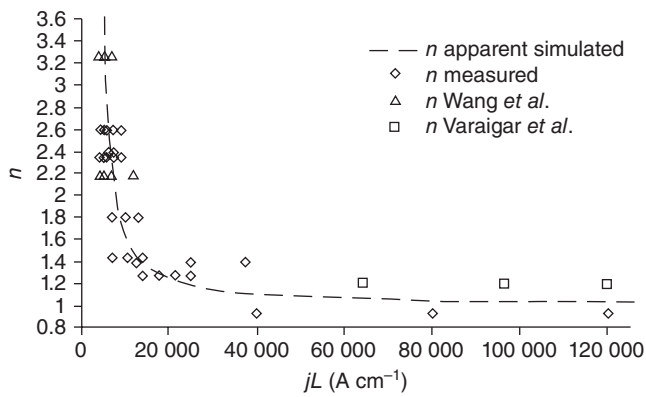
even totally annihilated. Such phenomena may occur in accelerated electromigration tests as well as in the product in operation. Extrapolation of interconnect lifetime requires an accurate determination of electromigration parameters, which means that any Blech effect should be de-correlated from current density acceleration before projection in operating conditions. Not only can the Blech effect induce an artificial extent of time in a test, but also a misleading determination of the current density exponent. Thus $n$ variation should be expected owing to the nucleation/growth regime, as reported by Lloyd,[6] but the Blech effect also affects the apparent value of the current density exponent, as reported by Ney *et al.*[26] in Fig. 1.7.

Ney reported variations in the published values of the current density exponent $n$ that perfectly match the known Blech effect. Similarly, Doyen *et al.*[29] reported continuous variations in the apparent value of the current density exponent, that are likely to affect lifetime projection. In Fig. 1.8, significant deviation from Black' law with $n = 1$ is measured for small current density owing to the Blech effect and high current density owing to nucleation and or Joule heating.

After careful determination of electromigration parameters, it is also possible to predict the Blech effect at operations conditions. Ney *et al.*[26] established a simple formalism, deriving from Black's equation, to take into account the Blech effect in lifetime projection. Not only does the Blech effect make interconnects smaller than a critical length immortal with respect to electromigration, but other short line lifetimes are extended owing to mass flux saturation.

Together with the accurate determination of the $j \times L$ threshold, it is important to evaluate the number of interconnect lines that are longer than the above mentioned critical length, as these represent potential electromigration failure locations. In practice, it is quite complicated to run a complete analysis of chip layout owing to the large number of segments.




*1.7* Evolution of apparent $n$ value with experimental $j \times L$ conditions.

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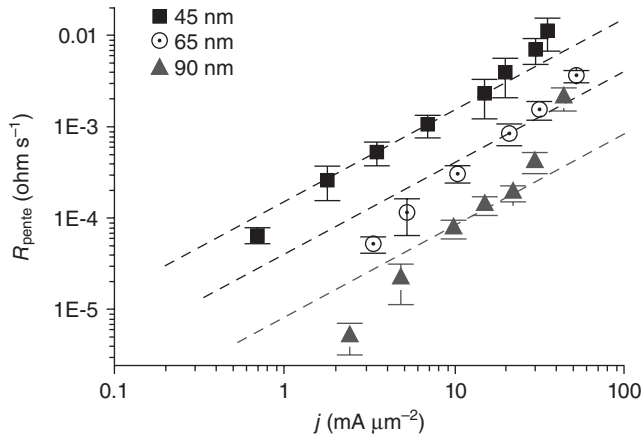
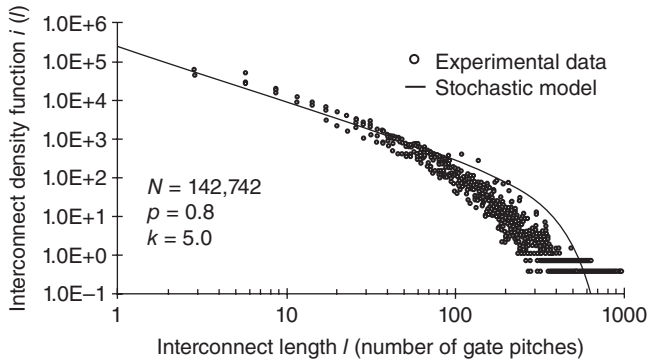



*1.8* Evolution of drift velocity with current density, dotted line corresponds to $n = 1$, for various technology nodes.




*1.9* Distribution of interconnect line length. See reference 30, J.A. Davis, A stochastic wire-length distribution for gigascale integration, *IEEE Trans. Electron Devices* **45**(3) (1998) 580–89. (© 1998 IEEE).

However, a stochastic model gives an estimation of the number of possible failures, and the scaling factor between interconnect failure rate and chip failure rate. The model proposed by Davis[30] expresses the possible combination of logic gates in a chip to create a distribution of necessary lengths to build the aforementioned logic function (Fig. 1.9). This simple model scales the occurrence of potentially failing sites as 1/1000 for a critical length of 100 μm.

## 1.3 Numerical methods

Early analytical equations of mass transport described in previous section give insights about electromigration behavior. However only a rough

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estimate of time to failure equation is given and the immortality criteria $(J \times L)_c$ can only be applied to simple cases, i.e. simple interconnect geometry. A one-dimensional analytical model is based on many simplifications, and, in particular, it does not take into account the four driving forces involved in the mass transport, nor the complex evolution of void shape during its growth.

Using a multiphysics approach, it is possible to take into account several driving forces to simulate electromigration. The finite element method (FEM) is an appropriate method to solve the case of physically coupled phenomena, such as conduction current, mechanical stress, temperature and diffusion.

As remarked by Tan and Roy,[31] there are two categories of FEM simulation. The first approach consists of a weak coupling calculation of flux divergence from one side and another degree of freedom (temperature, displacement, potential) from another side.[32,33,34] Basically, assuming a constant atomic concentration $N$, the total mass flux $J_\Sigma$ divergence is expressed by:

$$\begin{aligned}\operatorname{div}(J_\Sigma) = &\left( J_E \left[ \frac{E_a}{kT^2} - \frac{1}{T} + \alpha \frac{\rho_0}{\rho} \right] + J_T \left[ \frac{E_a}{kT^2} - \frac{3}{T} + \alpha \frac{\rho_0}{\rho} \right] \right. \\ &\left. + J_S \left[ \frac{E_a}{kT^2} - \frac{1}{T} \right] \right) \operatorname{grad}(T) + \frac{NQD_0}{kT^2} \\ &\exp\left( -\frac{E_a}{kT} \right) \frac{(j\rho q)^2}{3k^2 T} - \frac{2N\Omega D_0 E\alpha}{3kT(1-\nu)} \\ &\exp\left( -\frac{E_a}{kT} \right) \left( \frac{(j\rho q)^2}{3k^2 T} \left[ \frac{1}{T} - \alpha \frac{\rho_0}{\rho} \right] \right) \operatorname{grad}(T^2)\end{aligned} \qquad [1.25]$$

where $J_E$, $J_T$ and $J_S$ are, respectively, the electromigration, thermomigration and stress migration mass flux. $D_0$ is the self-diffusion coefficient, $\rho$ the resistivity, $\alpha$ the thermal conductivity, $Q$ the heat transport, $\Omega$ the atomic volume, $E$ Young's modulus, $\alpha$ the coefficient of thermal expansion and $\nu$ the Poisson coefficient. The temperature, stress and current fields are provided by FEM software and the divergence of $J_\Sigma$ is calculated by an external user routine. A positive mass flux divergence leads to void growth, whereas a negative mass flux divergence leads to hillock formation. If using ANSYS® software, the 'death birth' feature enables the user to delete elements of the system which have the highest mass flux divergence. Then a new static field is computed in the line that includes a void. Using this approach deleted elements of the FEM model correspond to the void shape as illustrated in Fig. 1.10. This strategy enables a quasistatic void growth simulation without accurate time to failure assessment because the mass transport equation is not solved.

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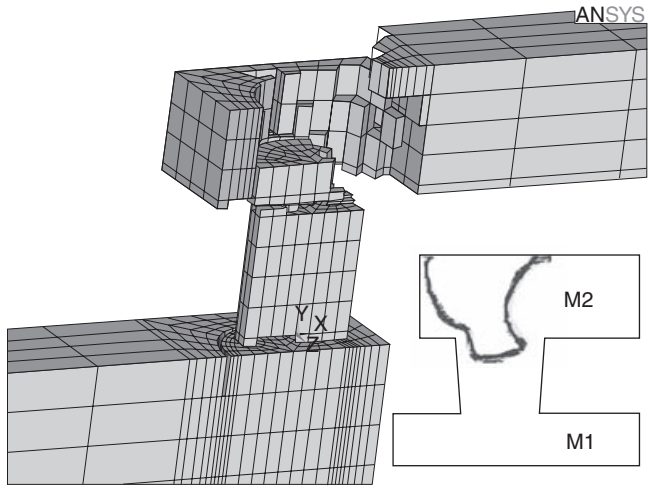


*1.10* Dynamical void growth.[34,36,38,39]

In the second approach,[35–37] all degrees of freedom are solved together. The first approach is numerically easier to handle because quasistatic void growth provides a rough approximation of critical location in the line but the kinetics of the problem are not well represented.

Electromigration, like most of the solid-state reactions or transformations, can be described as the succession of nucleation and growth process steps. The first step consists of vacancy diffusion, which leads to accumulation on the cathode side and depletion on the anode side. When the vacancy concentration (or the stress) reaches a critical value, a void nucleates. The characteristic time $\tau_d$ may not be measurable in practice, because it induces no effect on electrical properties of interconnects. There is no major change in the microstructure and the line resistance remains constant. The second step is the void growth. The resistance change is controlled by the void shape; in practice, measurable resistance change occurs when a growing void reaches the bottom of the metal line. Moreover, the diffusion barrier acts as shunt resistance, but as it is very resistive, a abrupt resistance step is usually recorded (Fig. 1.11).[38] The characteristic time is $\tau_f$, the time to failure, which is therefore a result of the diffusion rate and void shape.

In the following section, vacancy transport mechanisms are reviewed. The nucleation phenomenon is studied thanks to continuum physics, without using 'birth of void entities' concepts in the copper material, i.e. after reviewing the governing equation and the associated physics, some illustrative results are presented.

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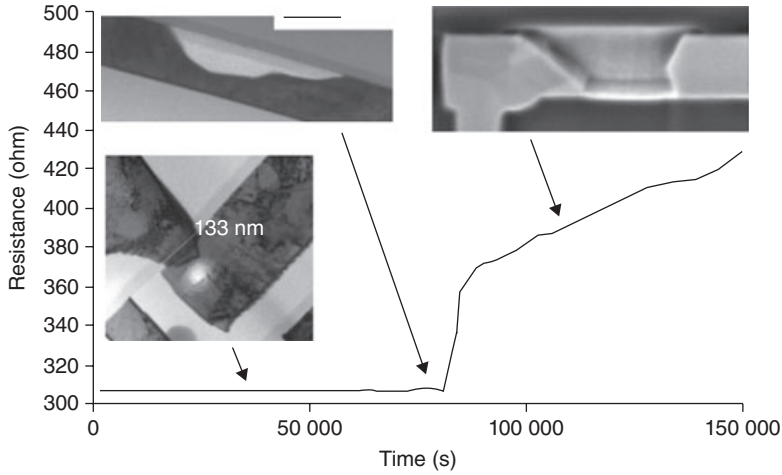


*1.11* Typical evolution of resistance during electromigration testing of copper interconnect, through various steps of void nucleation and growth. See reference 38, X. Federspiel, D. Ney, L. Doyen, V. Girault, Dynamics of resistance evolution during electromigration stress, IEEE International Integrated Reliability Workshop (2006), 24–27. (© 2006 IEEE).

### 1.3.1 Vacancy transport constitutive equation

Assumptions are similar to those from part 1.2.1. The microstructure of copper is not taken into account. As atomic diffusion is the result of a vacancy exchange mechanism, the effective vacancy diffusivity $D_v$ is given by:

$$C_a D_a = C_v D_v \qquad [1.26]$$

where $C_a/C_v$ and $D_a/D_v$ are, respectively, the concentration of vacancies/atoms and the diffusivity of vacancies/atoms. Typically, at 200 °C, the $C_v/C_a$ ratio is roughly $10^{-7}$.

The electron wind force alone is insufficient to quantitatively describe the mass transport. Other contributions are included in the electrochemical potential and is taken as:

$$\mu = \mu_0 + \mu_E + \mu_T + \mu_C + \mu_S \qquad [1.27]$$

where $\mu_0$, $\mu_E$, $\mu_T$, $\mu_C$ and $\mu_S$ are, respectively, the electrochemical potentials related to the reference state, electromigration, thermomigration, concentration and stress migration. The driving force $F$ derives from the electrochemical potential, $F = -\text{grad}(\mu)$, and the net vacancy flux $J_v$ along the line is a function of the driving force:

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$$J_{\mathrm{v}} = \frac{DC_{\mathrm{v}}}{kT} F \qquad [1.28]$$

The total vacancy flux $J$ is the sum of four contributions:

$$J = \sum_{\mathrm{i}} J_{\mathrm{i}} \begin{cases} J_1 = -D_{\mathrm{v}} \nabla C_{\mathrm{v}} \\ J_2 = -\dfrac{D_{\mathrm{v}} C_{\mathrm{v}}}{kT} Z^* e \nabla V \\ J_3 = -\dfrac{D_{\mathrm{v}} C_{\mathrm{v}}}{kT} f \Omega \nabla \sigma_{\mathrm{h}} \\ J_4 = -\dfrac{D_{\mathrm{v}} C_{\mathrm{v}}}{kT} \dfrac{Q^*}{T} \nabla T \end{cases} \qquad [1.29]$$

Adding the Fickian term $J_1$, the flux depends on the gradient of the hydrostatic stress $\sigma_{\mathrm{h}}$ ($J_3$), temperature $T$ ($J_4$) and potential $V$ ($J_2$). Assuming that a vacancy behaves like a substitutional foreign atom in the copper lattice, but with a smaller volume, the vacancy volume relaxation is given by the $f$ ratio in $J_3$. The transport heat $Q^*$ in $J_4$, is the isothermal heat transmitted by moving the atom in the process of jumping a lattice site.

Moreover, the generic form of vacancy diffusivity $D_{\mathrm{v}}$ is assumed to be characterized by an exponential dependence on the hydrostatic stress[39] and temperature:

$$D_{\mathrm{v}} = D_{\mathrm{v0}} \mathrm{e}^{\frac{(1-f)\Omega\sigma_{\mathrm{h}} - E_{\mathrm{a}}}{kT}} \qquad [1.30]$$

where $D_{\mathrm{v0}}$ is the prefactor and $E_{\mathrm{a}}$ is the activation energy of vacancy diffusion. The vacancy concentration is driven by a general diffusion equation, with $G$ a source/sink term:

$$\dot{C}_{\mathrm{v}} = -\Delta J_{\mathrm{v}} + G \qquad [1.31]$$

Usually, the source/sink term describes the production of vacancies when their concentration is larger than the equilibrium value whereas the opposite case describes the annihilation of vacancies:

$$G = -\frac{C_{\mathrm{v}} - C_{\mathrm{v0}} \mathrm{e}^{\frac{(1-f)\Omega\sigma_{\mathrm{h}} - E_{\mathrm{v}}}{kT}}}{\tau_{\mathrm{v}}} \qquad [1.32]$$

where $\tau_{\mathrm{v}}$ is the characteristic generation/annihilation time, $E_{\mathrm{v}}$ the activation energy of vacancy formation and $C_{\mathrm{v0}}$ the equilibrium vacancy concentration in the absence of stress and at zero kelvin.

Assuming that grain boundaries play an important role in the generation and annihilation of vacancies, Ceric *et al.* suggested another equation set.[40] The source/sink term $G$ is now expressed as a function of the incoming and outcoming fluxes through the grain boundary, respectively, $J_{\mathrm{v,1}}$ and $J_{\mathrm{v,2}}$, and $\delta$ the grain boundary thickness.

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$$G = \frac{J_{v,1} - J_{v,2}}{\delta} \quad [1.33]$$

where the incoming and outcoming fluxes are expressed by:

$$J_{v,1} = \omega_T (C_{veq} - C_v^{im}) C_v^1 - \omega_R C_v^{im} \quad [1.34]$$

$$J_{v,2} = -\omega_T (C_{veq} - C_v^{im}) C_v^{im} + \omega_R C_v^{im}$$

where $\omega_T$ is the trapping rate of vacancies in the grain core, $\omega_R$ the release rate, $C_v^{im}$ the trapped vacancy concentration and $C_{veq}$ the equilibrium vacancy concentration in the grain boundary. Finally the conservative mass balance from equation [1.31] is solved by coupling the corresponding current Laplace equation, [1.35], the equilibrium mechanical equation, [1.36], and the Fourier thermal equation, [1.37], as follow:

$$\nabla\left(\frac{1}{\rho}\nabla V\right) = 0 \quad [1.35]$$

$$\nabla\sigma = 0 \quad [1.36]$$

$$\nabla(k\nabla T) = -\frac{|\nabla V|^2}{\rho} \quad [1.37]$$

where $\rho$ and $k$, respectively, are the electrical and thermal conductivities. Equations [1.31], [1.35], [1.36] and [1.37], are solved simultaneously in the transient state. For numerical reasons, equation [1.31] is solved with normalized concentration $N$ in order to simplify the initial condition:

$$N = \frac{C_v}{C_{v0}} e^{\frac{E_v}{kT_i}} \quad [1.38]$$

$$N(t_i) = e^{\frac{(1-f)\Omega\sigma_{hi}}{kT_i}}$$

At the initial time $t_i$ (before applying current), the initial hydrostatic stress field is $\sigma_{hi}$ and the initial temperature is $T_i$.

## 1.3.2 Mechanical constitutive equation

The difference between the volume of an atom and the volume of a vacancy leads to a volumetric strain, similar to a thermal expansion-induced stress. In the general framework of small deformation formulation, the strain rate partition in an elementary volume is expressed as:

$$\dot{\varepsilon}^{tot} = \dot{\varepsilon}^{elast} + \dot{\varepsilon}^{ther} + \dot{\varepsilon}^{visco} + \dot{\varepsilon}^{em} \quad [1.39]$$

The total strain rate is the sum of the elastic strain rate, the thermal strain rate, the viscoplastic strain rate and the electromigration strain rate parts.

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After copper annealing, the cooling down to room temperature leads to a residual stress state owing to a coefficient of thermal expansion mismatch:

$$\dot{\varepsilon}_{ij}^{ther} = \alpha \dot{T} \delta_{ji} \quad [1.40]$$

where $\alpha$ is the coefficient of thermal expansion and $\delta_{ij}$ is Kronecker's symbol.

Several theoretical models have been proposed to describe electromigration-induced stress evolution. Initially, Povirk[41] and Rzepka *et al.*[42] considered that mass accumulation or depletion leads to the following strain rate.

$$\dot{\varepsilon}_{ij}^{em} = \Omega \nabla J \delta_{ji} \quad [1.41]$$

The Sarychev *et al.*[43] approach considers the source term. The electromigration strain rate part has two origins: the first is the vacancy flux divergence and the second is the vacancy generation/annihilation. Equation [1.42] expresses the diagonal tensor; a detailed demonstration was given by Sarychev *et al.*[43]

$$\dot{\varepsilon}_{ij}^{em} = \Omega[f \nabla J + (1-f)G]\delta_{ji} \quad [1.42]$$

It is assumed that when an atom moves under electromigration forces it leaves behind a vacancy. There is a local spherical symmetry strain field induced at that lattice site owing to the difference between the volume of an atom and the volume of a vacancy.

The last term in equation [1.42] is the viscoplastic part. Constitutive material behaviors of copper or aluminum have been investigated.[44,45] In a simple expression of Coble creep controlled by electromigration-induced grain boundary diffusion suggested by Li and Dong,[46] the creep rate dependence with current density is linear. More generally, viscoplasticity flow could be modeled by a power law of the von Mises stress invariant $M(\sigma)$, with a threshold $R_0$. With the convention $<a> = \max(a,0)$, the viscoplastic strain rate tensor is written as:

$$\dot{\varepsilon}_{ij}^{visco} = \frac{\partial f}{\partial \sigma} \left\langle \frac{f}{K} \right\rangle^{n} \quad [1.43]$$

where

$$\frac{\partial f}{\partial \sigma} = \frac{3}{2} \frac{s}{M(\underline{\sigma})}$$

$$f = M(\sigma) - R_0$$

and

$$M(\sigma) = \sqrt{\frac{3}{2} \underline{s} : \underline{s}}$$

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where $s$ is the deviatoric part of the stress tensor. The threshold $R_0$, $n$ and the parameter $K$ of the Norton law are temperature independent but $K$ could have a Arrhenius dependence.

For electromigration of solder alloys, Tang and Basaran,[47] Kashyap and Murty[48] and Basaran *et al.*[49] use the same form of viscoplastic flow with a kinematic hardening term because, in this case, fatigue loading and thermal cycling effects are significant. Extraction of material parameters for thin films as used in interconnects is quite challenging and a calibration of copper viscoplastic flow law is still not available. Thus, the viscoplastic part is not included in the following development. However, it has been highlighted that plasticity build-up, more precisely dislocation cores, play an important role as fast diffusion paths. The so-called 'pipe diffusion' would amplify diffusivity, and thus affect the MTF.[50]

Sarychev's work inspired various studies[51,52] and it enables stress evolution to be simulated in two-dimensional (2D) structures, where a homogeneous diffusion medium without any preferential diffusion path is considered. Sukharev *et al.*[53] and Sukharev[54] distinguished the different diffusion paths for the interface and the bulk. They assumed two different vacancy concentrations $C^{\text{int}}$ and $C^{\text{bulk}}$, and thus two continuity equations are solved:

$$\frac{\partial C^{\text{bulk}}}{\partial t} + \nabla J^{\text{bulk}} = 0 \quad \text{and} \quad \frac{\partial C^{\text{int}}}{\partial t} + \nabla J^{\text{int}} = G^{\text{int}} \qquad [1.44]$$

The interface means the grain boundaries, the interface Cu/SiN, the diffusion barrier Ci/TaNTa for which a higher diffusivity coefficient $D_v$ is imposed than the bulk one. Plated atoms are exchanged between bulk and interface, so vacancy generation or annihilation is represented by atom plating or removal from the grain boundary. The source/sink has a standard form:

$$G^{\text{int}} = \frac{C_v^{\text{int}} - C_{\text{eq}}}{\tau} \qquad [1.45]$$

If we are considering that the plated atoms are immobile and are defined by a concentration $C_a$, the plated atom continuity equation for bulk and interfaces is given by:

$$\frac{\partial C_a^{\text{bulk}}}{\partial t} = 0 \quad \text{and} \quad \frac{\partial C_a^{\text{int}}}{\partial t} = G^{\text{int}} \qquad [1.46]$$

Sukharev[56] suggested that the diagonal term of electromigration-induced strain tensor is expressed by:

$$\varepsilon_i = \Omega \left[ (f-1)(C_v^{\text{int}} - C_{v0}^{\text{int}}) + (C_a - C_{a0}) \right] \delta_{ii} \qquad [1.47]$$

where $C_{a0}$ is the concentration of atoms in the plated copper layer without mechanical stress. Sukharev concludes that the evolution of atom concen-

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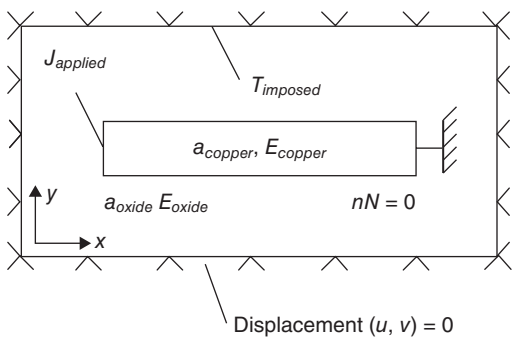
tration in the plated layer is mainly responsible for stress build-up. However, such an approach implies the resolution of several degrees of freedom, $C_v^{int}$, $C_v^{bulk}$ and $C_a^{int}$. The definition of the interface domain with a representative thickness is a strong limitation to this modeling strategy. Meshing fine domain with a high aspect ratio thickness/surface is known to induce a very large number of elements in FEM problems, this approach seems to be limited to 2D problems.

### 1.3.3 Application to evolution of stress in metal lines

*Model and boundary conditions*

A 2D FEM model is used to simulate vacancy transport in a copper line embedded in oxide. The electromigration testing conditions are representative of a package level test: the sample is maintained at uniform temperature, stress current density being small enough so that Joule heating and the subsequent temperature gradient in the system is not significant. As depicted in Fig. 1.12, in the present simulation, boundary conditions and initial conditions are set as follows:

- A current density in copper is set to 1 MA $cm^{-2}$. The temperature gradient is neglected and conductivity is assumed to be constant.
- Temperature is set to 340 °C in the external domain of the oxide.
- The system is assumed to be in a plane strain state. An initial hydrostatic stress state of 100 MPa (owing to a mismatch of thermal expansion coefficients between copper and oxide) is assumed at the considered temperature.
- Concerning vacancy diffusion, Neumann conditions at the copper/oxide interface are set in order to ensure the conservation of the total number of vacancies $N$. Effective copper diffusivity is assumed to be




*1.12* Schematic illustration of the boundary conditions for various degrees of freedom: temperature, current and displacement.

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constant in the whole structure. Equation [1.38] gives the field of initial concentration.

*Results*

Simulated evolution of stress and relative vacancy concentration are now presented for both 20 and 200 μm length copper lines. The results should be considered as qualitative. Moreover, the proposed model simulates stress evolution disregarding nucleation steps. However, the results of this simulation allow to evaluate the relevance of hypothesis of simpler models presented previously. First, despite the fact that the problem is formulated in two dimensions, the vertical total flux $J_y$ is negligible compared with $J_x$ as shown in equation [1.29]. As a consequence, the actual model could be reduced to a one-dimensional (1D) problem. Moreover, in such conditions, the four driving forces described in equation [1.29] do not act with the same weight:

$$|J_4| << |J_1| < |J_2| \approx |J_3| \qquad [1.48]$$

Therefore, qualitatively, at the cathode, high vacancy accumulation occurs, whereas there is depletion at the anode. Moreover, the hydrostatic back stress becomes increasingly tensile at the location of vacancy accumulation and it is more compressive at the location of vacancy depletion. Because of the low stiffness of oxide, stress in copper is partially relaxed in the vicinity (<1 μm) of the copper/oxide interface, therefore a stress gradient and concentration gradient develops from the center to the edge of the line. However, from the early beginning of diffusion, an equilibrium occurs at the cathode, so that this area, which is initially in depletion, starts to accumulate vacancies.

The evolution of stress in the 20 and 200 μm lines is shown, respectively, in Figs. 1.13 and 1.14, with the same time scale, i.e. $\delta = 1000$ s. For short lines, the back stress flux soon compensates the electromigration flux, and the steady state is reached. The steady state is reached when only a small amount of metal is effectively diffused, so that no void big enough to induce electrical failure is formed; this situation is referred to as 'immortality' behavior according to the Blech approach. On the other hand, for long lines, the stress drastically rises and reaches a critical value, thus allowing void formation and growth. However, it is likely that the void nucleation would locally modify the boundary conditions of the problem. The void nucleation stress is estimated to be 40 MPa for copper[55] and 500 MPa for aluminum.[56]

The evolution of the concentration $N$ at the cathode is summarized in Fig. 1.15 for two line lengths (20 and 200 μm), and two current densities (1 and 3 MA cm$^{-2}$). At this location, the stress is partially relaxed and so $N$ is close to one. A small current density in a small segment leads to a very low

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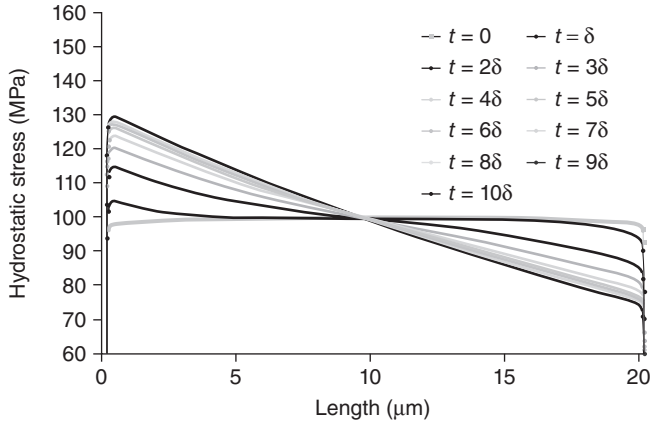
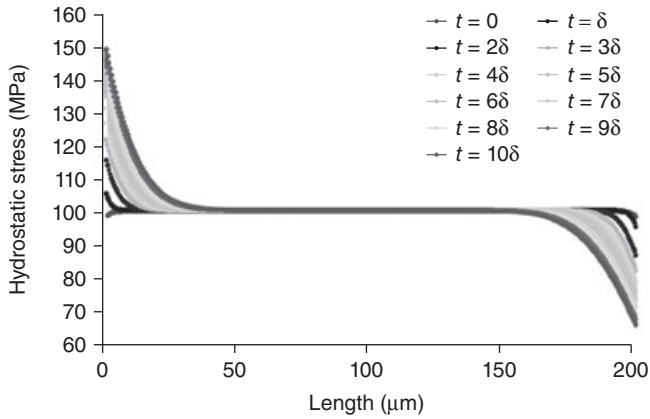



*1.13* Hydrostatic stress evolution in a 20 μm length copper line; the left side is the cathode.




*1.14* Hydrostatic stress evolution in a 200 μm length copper line; the left side is the cathode.

value of vacancy saturation, as the steady state is reached. In a given segment, when increasing the current, the accumulation is enhanced and occurs earlier. Moreover, for a long segment, $N$ may be increased by a factor 10, because the total vacancies $N_t$ available for diffusion is much more important.

An in-depth analysis of Fig. 1.14 shows that the stress field is not perfectly symmetric. This can also be observed in concentration distribution, which is not precisely shown here. On the other hand, migration kinetics are slightly accelerated at the cathode and slowed down at the anode. This subtle difference results from stress diffusivity dependence, see equation

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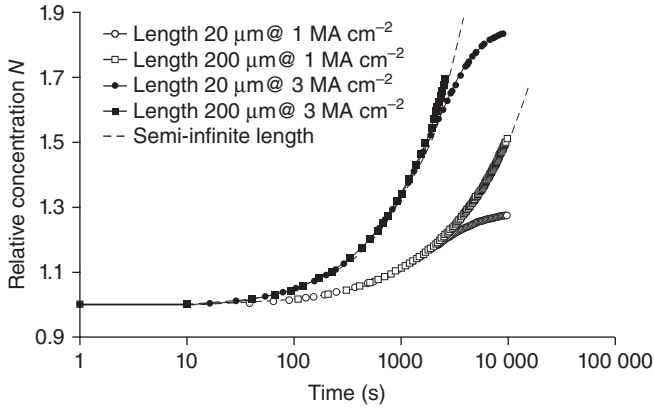


*1.15* Evolution of the concentration *N*, at the cathode for two segment lengths and two current densities.

[1.30]. This model is rather simplified: the diffusion paths, the texture-induced stress localization and the current concentration under via are not taken into account here and will be analyzed in a later section.

### 1.3.4 Application to real circuit layout case

In this section, we present a 2D simulation of a real circuit layout and analyze the consequences of the Blech effect on circuit lifetime and dc current design rules. Moreover, dc electromigration rules, as used in semiconductor industries, are commonly described as maximum current allowed in a metal line with vias at each end. The maximum current in operation is fixed disregarding the number of connections to this line as well as any variation of current along the line. As described in the previous section, the Blech effect is likely to slow down or totally stop the electromigration flux when the $j \times L$ product is under a certain threshold. This picture is simple to analyze in an elementary line under constant current but it is not directly applicable to complex interconnection.

As an example of a complex interconnection tree, we defined a simplified model of a power grid where the main line is feeding current to various blocks connected along the line through single vias (see Fig. 1.16). Several cases were simulated, making the number of vias along the line varying, as well as changing the current i.e., constant current density in feeding vias (line end) or constant current in vias connected to blocks ($J_{\text{applied}}$ in Fig. 1.16). Simulation results for the vacancy concentration profile in the line for the stationary regime are plotted in Fig. 1.17. The hazard of electromigration failure is assessed according to the vacancy profile or stress profile. The nucleation and growth of a void is not taken into account, but

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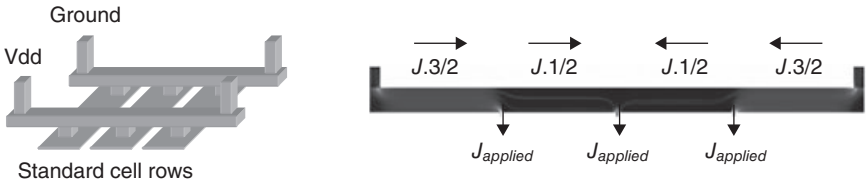
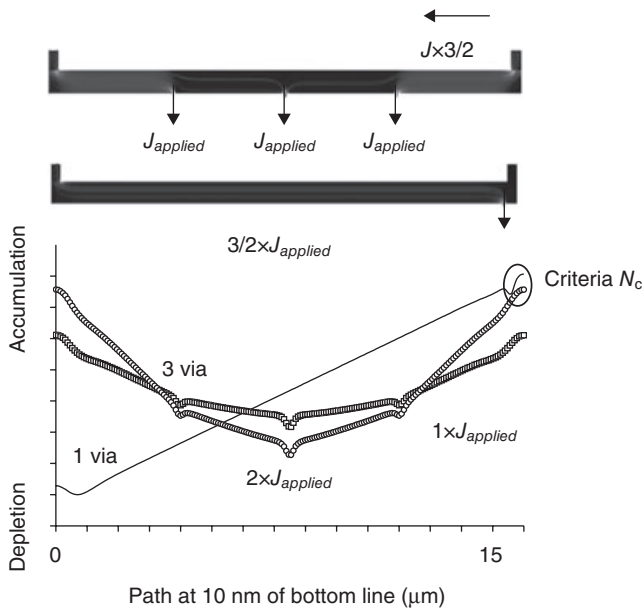



*1.16* Illustration of simplified power grid layout, line M1 is supplied by two stacked vias (left). Vacancy transport is simulated in line M1 assuming that all contacts delivered the same current $J_{applied}$ (right).




*1.17* Comparison of vacancy profile in single metal line and power grid case, for constant feeding current and total length.

the evolution of vacancy concentration is interpreted as the amount of potential void volume. Using this figure of merit, we compared a simple metal line with a power grid.

From Fig. 1.17, it appears that the maximum vacancy concentration is lower in the power grid than in the simple line case. In other terms, the effective length corresponding to the Blech effect is not the total line length, but rather depends on the local current density and flux divergence. As a consequence, the dc current rule could be relaxed by a certain factor after accurate simulation of the real layout.

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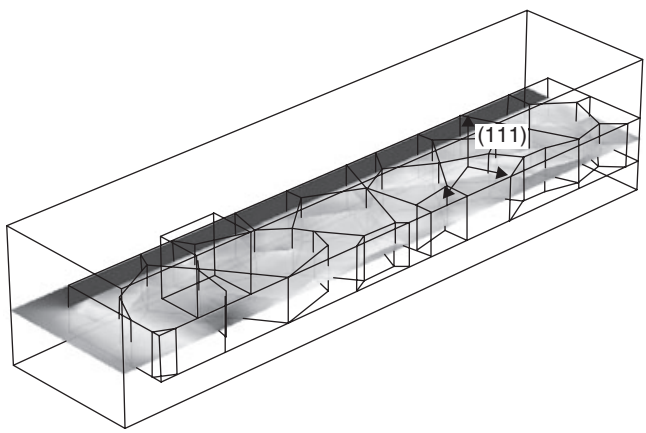
### 1.3.5 Application to diffusion path and texture effects

*Model and boundary conditions*

The purpose of this three-dimensional (3D) model is to simulate electromigration in a metal line containing a significant number of copper grains whose crystalline orientation reflects the (111) texture, i.e. the copper grains are (111) oriented along the *z*-axis and randomly oriented in the plane *x*-*y*. Grain size is set to the order of line width to simulate the 'bamboo' case, and line length is set to 2 μm, which means that the line is 'immortal' with respect to the usual Blech criteria. The line is embedded in dielectric and connected to metal vias so that mechanical and electrical 3D effect can be simulated. Copper has a fcc structure and its elastic properties are defined thanks to three constants, like any cubic element: $C_{11} = 168$, $C_{12} = 121$ and $C_{44} = 75$ GPa.

At the temperature of the electromigration test, the thermal expansion between the oxide and the copper leads to a large inhomogeneity in the shear stress state owing to the anisotropic elasticity use. Indeed, strong grain disorientation leads to an important stress gradient, including a zone in compressive stress, whereas the average stress is tensile. The Von Mises stress state before applying current is shown in Fig. 1.18. Moreover, the gradient of stress and current density concentration are particularly high at the vicinity of the via/line interface. In this location, the current crowding creates an electromigration flux divergence, which is also a mechanical singularity at the interface copper line/via.

The copper/capping interface has been reported as a fast diffusion path for electromigration.[57] However, in this model, all the possible different diffusion paths are taken into account, i.e. the copper/capping interface, the




*1.18* Map of von Mises component in cross-section of a copper line before the current stress. Grains are (111) textured.

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copper/diffusion barrier interface, the grain boundary and bulk diffusion and are noted as 1, 2, 3 and 4 in the following. Equation [1.31] with $D_{v4}$ and the boundary conditions involve the diffusivity $D_{v1}$, $D_{v2}$ and $D_{v3}$. In practice, the diffusivity coefficient is quite difficult to measure, because it is highly dependent on the impurities concentration and process parameters. However, the activation energy is found to be 2.15 eV for bulk copper,[39] 1.2, 0.92 and 0.85 eV for the grain boundary[57–59] and 1.06, 1 and 0.8 eV for interfaces.[60] In our model, diffusivity prefactors are set as following:

$$D_{v1} = 1000 D_{v4}$$

$$D_{v2} = 800 D_{v4}$$

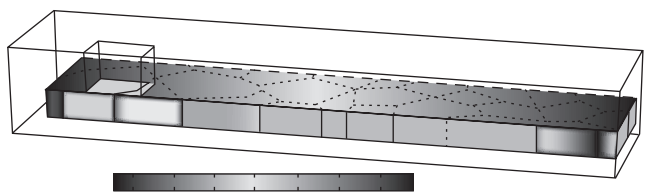
$$D_{v3} = 500 D_{v4}$$

The first diffusion paths are the copper/capping and copper/diffusion barrier interfaces. The ratio between all diffusion paths is consistent with reported nucleation of electromigration voids. Moreover, void nucleation is frequently reported to occur next to the via at the triple point between, the barrier/copper and the copper/capping interface, where a strong flux divergence is expected to occur.

*Results*

In the initial condition, the concentration $N$ is quite constant inside the line; indeed the hydrostatic stress is quite homogeneous. Then, concentration quickly increases in paths 1, 2 and 3, and finally bulk grain concentration is affected.

Because of the field of vacancy concentration shown in Fig. 1.19, vacancy accumulation occurs at the cathode, through paths 1, 2 and 3, whereas grains under the via are close to equilibrium concentration $N \sim 1$. In addition, it is remarkable that the grain boundary under the via, which is perpendicular to the line and main transport direction, plays an important role in vertically carrying vacancies from the bottom of the interface towards the via.




*1.19* Field of vacancy concentration in the line in transient state, diffusion follows different paths: interface, grain boundary and lattice.

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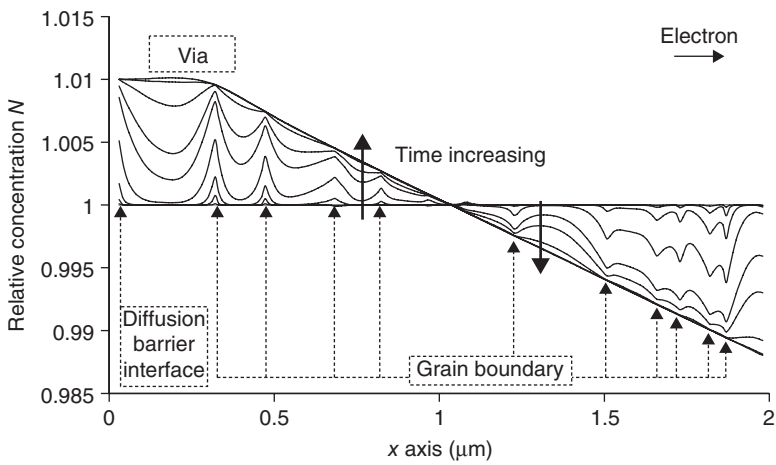
Although path 4 (bulk) plays a minor role in the transient regime, and is not a limiting factor for the overall electromigration dynamics, it eventually controls the concentration gradient inside grains. In Fig. 1.20, we plotted vacancy concentration across several grains, for different time steps. The concentration profile shows sharp oscillation through neighboring grains that converge to form a smooth profile in a steady state value. The concentration gradients are sharper in small grains than in large grains. The grain boundary and the interfaces act as sink/sources for vacancies to maintain concentration in the bulk at the equilibrium. In other words, $G$ described in equation [1.32], should be rewritten for the different diffusion paths with a characteristic time following: $\tau_1 < \tau_2 < \tau_3 << \tau_4$.

## 1.3.6 Morphological void evolution

The dynamics of electromigration-driven void growth in solid metals is a wide research field and a challenging theoretical problem.[61] Capillary forces as well as electrostatic and electro-mechanical forces are involved in interface motion and morphology evolution. Various aspects of void morphology evolution are reviewed in the literature,[62–66] the electron wind promotes the formation of slit-shape voids, whereas surface driven void growth leads preferentially to round shapes. Therefore, the final shape will result from the initial shape as well as surface diffusivity and surface free energy. The evolution of void shape involves different processes, as its migration along the line is affected by the microstructure, with subsequent growth and collapse or the agglomeration at a particular location. Although fundamental




*1.20* Evolution of the vacancy concentration $N$ along the $x$ direction in the middle of the line at various steps time.

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understanding of void dynamics remains difficult, we review two types of interface modeling approach. In the first approach, the interface in the solid is represented as the ideal perfect sharp boundaries for which the front (interface void/metal) is explicitly computed and updated. In the second approach, an implicit function represents a smooth interface.

*Sharp interface approach*

The void motion is controlled by an atomic diffusion process along the void/metal interface. The diffusion of atoms lying on the crystal surface, known as adatoms, is faster than bulk diffusion. The chemical potential of an adatom in the interface is

$$\mu = \mu_0 - \Omega\gamma\kappa + Z^*eE \qquad [1.49]$$

where $\mu_0$ is the reference value of the potential, $\Omega$ is the atomic volume, $\gamma$ is the interface energy, $\kappa$ is the local curvature of the interface, $Z^*e$ is the effective charge and $E$ is the electrical applied field. The atomic flux along the interface is caused by the gradient of the chemical potential:

$$J_s = \frac{D_s\delta_s}{kT}\nabla_s\mu = \frac{D_s\delta_s}{kT}\left(\Omega\gamma\frac{\partial\kappa}{\partial s} - Z^*eE_s\right) \qquad [1.50]$$

where $\nabla_s$ is the surface Laplacian, $\delta_s$ is the interface thickness, $D_s$ is the interface diffusivity, and $E_s$ is the tangential electrical field to the interface. The normal velocity is then expressed by:

$$v_n = -\nabla_s J_s \qquad [1.51]$$

This last equation implies mass conversation and thus the conservation of the void size during important morphological void changes.[62]

Early analytical solutions provide asymptotical behavior. Assuming isotropic material properties and an infinite metal line, the analytical solution to this problem show that the motion velocity of a spherical inclusion is proportional to the applied electrical field and inversely proportional to the void size.[67] For a circular void shape, the normal velocity is given by:

$$v_n = 2\frac{D_s\delta_s}{dkT}Z^*eE_0 \qquad [1.52]$$

where $d$ is the void diameter, and $E_0$ is the applied electric field. The same development was established by Li and Chen for an elliptical void.[68] More general formulations are developed including diffusion anisotropy and current crowding owing to confinement.[69] However, numerical methods are preferred for modeling the void evolution. As mentioned before, sharp interface modeling implies that the function describing the interface void/metal is explicit and special techniques are used for the front tracking.

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Kraft and Arzt[70] used a numerical scheme which combined the FEM and the finite difference method (FDM). The FEM provides the temperature, whereas electrical field near the void and FDM provides the front normal velocity. The remeshing and field transfer procedure is performed iteratively. The assumption of constant void size means that there is no species exchange between the void/metal interface and mass transport inside the line. Consequently, the simulation is independent of line length therefore unable to reproduce the Blech effect. Kraft uses another definition of normal velocity which does not imply volume conservation. A low growth rate leads to slit-like voids whereas for higher rates it leads to wedge-shaped voids.

This modeling approach was improved for introducing anisotropic diffusion.[71] Indeed, simulation by the first principles method shows that the diffusion barrier energy of adatom on copper (001), (110) and (111) surface is, respectively, 0.68, 0.56 and 0.07 eV.[72] More recently, the dynamic response of the void morphology driven by surface electromigration was investigated and the effect of the electrical field, surface diffusion anisotropy and void size was examined.[73,74] The anisotropy of the surface adatom diffusivity is expressed by:

$$D_s = D_{s,\min}\{1 + A\cos^2[m(\theta + \phi)]\} \quad [1.53]$$

where $D_{s,\min}$ is the minimum surface diffusivity and $\theta$ is the angle between the local tangent to the void surface and the applied field direction. $A$, $m$ and $\phi$ are parameters that, respectively, determine the magnitude of the surface diffusivity anisotropy, the degree of anisotropy and the misorientation of a symmetry direction of fast surface diffusion with respect to the electrical field direction. Following the magnitude of the different contributions (electrical field, surface diffusion anisotropy or void size), some transitions from steady state to stable oscillatory morphological evolution can exist.[75] These transitions are the results of Hopf bifurcation at the corresponding critical point. The nature of the Hopf bifurcation is determined by the symmetry of the surface diffusion anisotropy and the bifurcation is supercritical and subcritical for fourfold ($m = 2$) and twofold ($m = 1$) symmetry, respectively. In addition, in symmetry cases, hysteresis phenomena and bistability was simulated. Illustration of different void morphological evolutions is presented in Fig. 1.21. The evolution of void surface area with particular model parameters has a oscillatory behavior and may be suddenly unstable.

Another point is the mechanical stress effect on the evolution of void morphology.[76] The normal velocity is modified to:

$$v_n = \frac{D_s\delta_s}{kT}\left(\Omega\frac{\partial^2 w}{\partial s^2} + \Omega\gamma\frac{\partial^2 \kappa}{\partial s^2} - Z^* e j_s\right) \quad [1.54]$$

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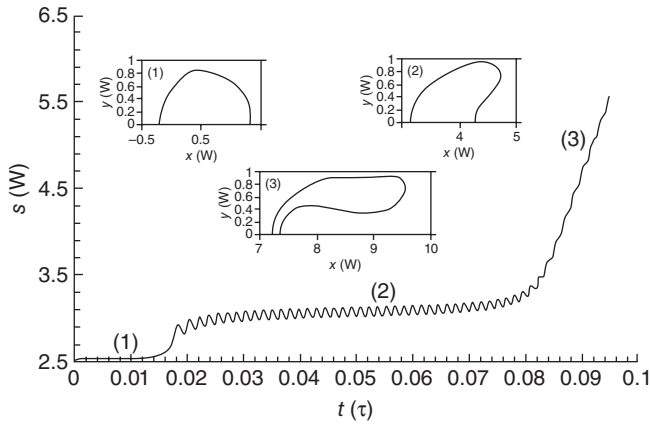


*1.21* Evolution of void surface area per unit film thickness *s* from an initial configuration with semi-circular cross-section on the plane of the film. The insets to the figure show void morphologies representative of the three stages in the void morphological evolution, (1), (2) and (3), characterized by the absence of surface oscillations, oscillatory dynamics, and the necking instability.[75]

where $w$ is the elastic energy density derives from a FEM solution. The consequence is that an initial circular void remains circular if the surface energy $\gamma$ has an important weight. On the other hand, if the electromigration term or elastic density energy is the major contributor, the void may collapse into a slit or present severe instability. Application with 3D simulation was demonstrated by Zhang.[77]

The interaction between grain boundary diffusion and void motion was simulated by Bower and Shankar[78] with a sharp interface approach. The model includes grain boundary sliding, grain boundary diffusion, grain boundary migration and surface diffusion. According to the gradient of chemical potential, atoms can detach from the grain, diffuse along the boundary and re-attach to another grain or surface. The flux of the atoms tangent to each interface is the same as in equation [1.50] but the gradient of the normal stress component to the boundary is added. Several phenomena were simulated; the void may remain connected to the grain boundary while both the void and grain boundary migrate together down the line; the void may migrate and detach from the grain boundary; the void may grow or shrink, while migrating with or without the grain boundary. For the sake of illustration, the case of a void released from a grain boundary[79] is shown in Fig. 1.22. The surface evolves much faster than the grain boundary and consequently the void de-pins from the grain boundary. On the other hand if the surface and the grain boundary migrate at similar rates the void remains pinned at the grain boundary.

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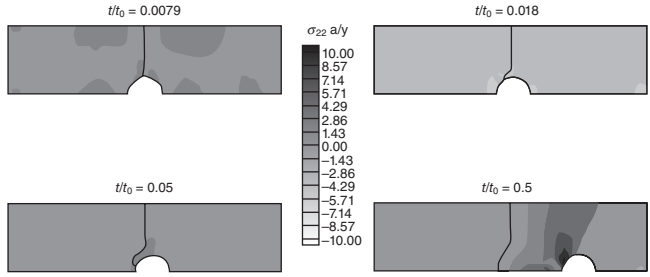


*1.22* Void escaping from a grain boundary.[79]

Finally, the shape interface method is attractive for describing complex void shape dynamics. Its enables us to accurately investigate the consequence of a local property of the interface on the void surface evolution. However, the explicit function of the interface needs to be continuous whatever the evolution of the void (bistability, void collapse, etc.). Front tracking is generally difficult to handle, it may require re-meshing and field transfer procedures. While this method is efficient for 2D geometry, the generalization to 3D geometry is challenging.

*Diffuse interface approach*

In the diffuse interface approach a phase field is solved and the interface corresponds to the zero contours of the phase field. Thus, the void surface is implicitly represented by an order field parameter. The field parameter $\phi$ takes the value –1 and +1, respectively, in the solid and void phase. It has a smooth evolution inside the interfacial medium between the two phases. The evolution of the phase field is governed by the Cahn–Hilliard equation. Some illustrations have been proposed.[79–81] It is noticeable that the adaptative mesh procedure is necessary during the simulation, fine element size is needed in the narrow interfacial domain and the element size is relaxed elsewhere for the computation of the mechanical and electrical fields. This strategy seems to be very resource consuming and not adequate for 3D geometry. The level set method is preferable. The idea of evolving an interface by representing it as a level set of a field function was introduced by Osher and Sethian.[82] The interface $\Gamma$ is implicitly represented as the one half level of a continuum function $\phi$. The interface is defined as follows:

$$\Gamma = \{x|\phi(x, t) = 0.5\} \qquad [1.55]$$

where the $\phi$ function ranges from 1 to 0, that corresponds respectively to the metal and the void phases. With the normal velocity $v_n$ of the interface, $\phi$ evolution is given by a Hamilton-Jacobi equation:

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$$\dot{\phi} + v_n |\nabla \phi| = 0 \quad [1.56]$$

Shape change or drift along the metal line of the void surface is caused by adatom diffusion. The interface velocity caused by electromigration flux is usually assumed to be proportional to the component of the electrical field tangent to the surface and the chemical potential gradient along the void surface. Assuming mass conservation, the normal component of velocity at any point of the surface is given by:

$$v_{\mathrm{n}} = -\frac{\partial}{\partial s} D_{\mathrm{s}} \left[ \Omega \left( \frac{\partial \gamma \kappa}{\partial s} \right) + Z^* e \frac{\partial V}{\partial s} \right] \quad [1.57]$$

where $\gamma$ is the surface energy, $\kappa$ is the local curvature of the surface and $s$ is the interface arc length. With this formulation of normal velocity, the shape of the initial void was investigated and it was demonstrated that the electric field strength drives the morphology of the void, and that at higher current density, slit-like shape voids may occur. Note that $\gamma$ and $D_{\mathrm{s}}$ may be anisotropic, and the details are available in other studies.[83]

Another definition of $v_{\mathrm{n}}$ is preferred. Indeed, the major drawback of equation [1.57] is that no exchange between adatom diffusion in the void surface and the vacancies in the metal line is considered. To circumvent this limitation, a coupling between the vacancy transport equation and the surface motion is performed. Hence, the vacancy flux $J^{\mathrm{s}}$ at the void surface $s$ is expressed as:

$$J^{\mathrm{s}} = \sum_{\mathrm{j}} J_{\mathrm{j}}^{\mathrm{s}} \begin{cases} J_1^{\mathrm{s}} = -\dfrac{D_{\mathrm{v}}^{\mathrm{s}} C_{\mathrm{v}}}{kT} Z_{\mathrm{s}}^* e \nabla_{\mathrm{s}} V \\ J_2^{\mathrm{s}} = -\dfrac{D_{\mathrm{v}}^{\mathrm{s}} C_{\mathrm{v}}}{kT} \gamma \Omega \nabla_{\mathrm{s}} \kappa \end{cases} \quad [1.58]$$

$\delta(\phi)$ is the smooth $\delta$-function of $\phi$, $\nabla_{\mathrm{s}}$ is the surface gradient operator, the global vacancy diffusivity can be rewritten:

$$D_{\mathrm{v}} = \delta(\phi) D_{\mathrm{v}}^{\mathrm{s}} + \phi D_{\mathrm{v}}^{\mathrm{lattice}} \quad [1.59]$$

The diffusion equation is modified in order to consider the interface flux $J^{\mathrm{s}}$:

$$\dot{C}_{\mathrm{v}} = -\phi \nabla J - \delta(\phi)\ \nabla_s J^{\mathrm{s}} + \phi G \quad [1.60]$$

Finally, the normal velocity depends on the local vacancy concentration rate:

$$v_{\mathrm{n}} = -\mathrm{sign}\ (N - N_0)\ K |\dot{N}| \quad [1.61]$$

where $K$, a physics-based constant, is temperature independent and arbitrarily set in the model. At the void interface, if the vacancy concentration reaches a yield value $N_0$, the normal velocity becomes negative. As a

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consequence, a concave or convex interface tends to respectively grow or shrink the void. The classical formulation of the interface velocity, as defined in equation [1.57], and the velocity based on vacancy concentration rate equation [1.61], may provide distinct void shape results.

In the next section, the model using equation [1.61] is applied to a practical case of electromigration in a copper line. However, for the sake of simplification, the drift of voids is not addressed. Therefore, assuming that $v_n = \min(v_n, 0)$, only the irreversible process of void growth is simulated.

*Application to void growth*

After discussing void dynamics, the aim of this application is to investigate the electrical signature during void growth. For the sake of simplification, a 2D model is built. The copper line length is 250 μm and grains are not explicitly represented. The fastest diffusion path is represented by the capping layer. The electrical conductivity of the 6 nm diffusion barrier is described; and the ratio between the resistivity of the diffusion barrier and copper is assumed to be 170. The package level test is performed at 300 °C, and the applied current density is 3 MA $cm^{-2}$.

The evolution of the simulated void growth, Fig. 1.23, and the electrical resistance change, Fig. 1.24, are simultaneously discussed:

- After a first step of vacancy transport suggesting void location, a small void is artificially introduced in the capping layer at a distance of 80 nm in front of the via, as seen in Fig. 1.23b at time $t_0$. No significant resistance change is observed during this period (Fig. 1.24).
- Then, at time $t_1$, the front grows in both vertical and lateral directions. As a consequence, the electrically conducting section is reduced, and hence the resistance smoothly rises.
- Once the bottom front of the interface reaches the diffusion barrier, the global line resistance drastically rises as shown in time $t_2$. Indeed, the electrical resistivity of the diffusion barrier is much higher than the copper one.
- Finally, the void grows at the side where vacancies are released by the capping layer. However, the other side of the front cannot move because vacancies do not have any diffusion path to reach this front. Time $t_3$ and $t_4$ correspond to a linear resistance rise; the slope of this regime enables a direct measurement of the drift velocity and can be used to determine the activation energy and the current density exponent.

Some observations of voids on different samples are presented in Fig. 1.23a: the case of an initial void located under the via (see Fig. 1.23a1) leads to an abrupt resistance rise and to a short-circuit in the conducting line, because the electrical path is not available anymore. Otherwise, the void is

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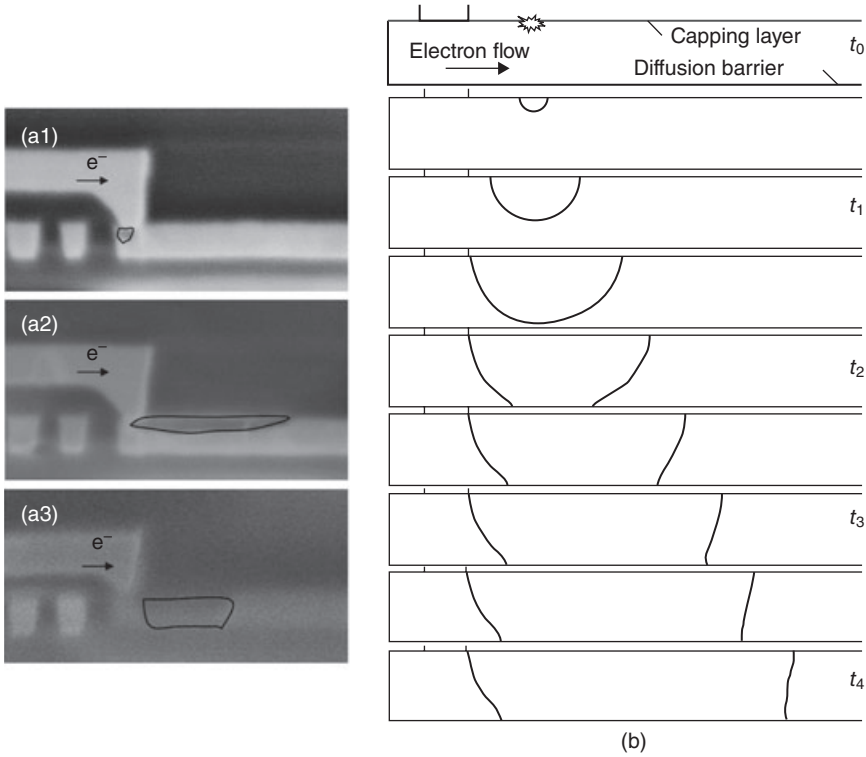
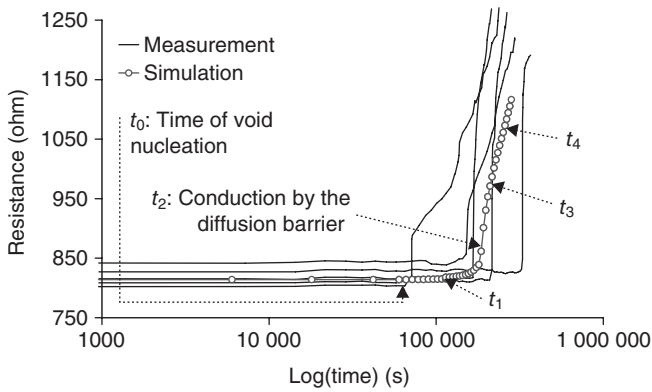



*1.23* (a) Cross-section of void in copper for various samples at the same time of electromigration test; (b) sequence of simulated void growth at different times of electromigration test.




*1.24* Evolution of the resistance during the electromigration test. The different lines represent a set of experimental measurements.

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usually nucleated in the capping layer in front of the via and grows both vertically and along the capping layer interface (see Fig. 1.23a2 and Fig. 1.23a3).

However, the electrical signature of a measurement set is not as simple as the one found in the simulated case. Indeed, several mechanisms, such as void coalescence and void trapping, which are not represented by the model, play an important role. Moreover the dispersion in terms of failure times, attributed to texture effects and process variability is not addressed.

## 1.4 Conclusion

From the simplest phenomenological MTF expression to the more sophisticated multiphysics simulations, the different modeling techniques are reviewed. The analytic solutions provide the profile of the hydrostatic stress or vacancy concentration along the line, regarding different assumptions of the vacancy generation and annihilation term in the grain core or in the grain boundary. For a time to failure limited by nucleation or growth, this approach can only be applied on a simple system. However, the basic nucleation criteria, which have not been developed here, remain rather complex to experimentally characterize. With the help of CPU resource democratization, simulations based on multi-driving forces have emerged in the past few years. Different numerical schemes have been developed for simulating the evolution of void shape during electromigration. Correlation with the electrical resistance profile makes the simulation qualitatively correct with regard to the time scale and the final void size.

Simulation of electromigration is a field under development and it is noticeable that new promising approaches are emerging. Physics-based predictive Monte Carlo simulation is able to model void incubation, its coalescence and void growth,[84] a physical MTF formulation being derived. Atomistic Monte Carlo simulation is suitable to deal with interatomic interaction under electromigration[85] or atomic drift/diffusion in the grain boundary.[86] Interestingly, the shape evolution of a void simulated by continuum theory matches the one given by kinetic Monte Carlo simulation in certain conditions.[87] The peridynamic approach has been recently derived from the multiphysics simulation of electromigration. Contrary to the classical continuum mechanics and transport equation, this approach has the advantage that the response fields do not need to be differentiable, and it is well adapted to handle the boundary conditions at the void surface.[88]

With the increasing complexity of models, the number of unknown parameters is becoming important. There are many parameters of the models that are difficult to address experimentally, such as interface proper-

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ties, effect of microstructure and texture. Consequently, simulation is difficult to calibrate and so models are still not able to predict time to failure. Moreover, the simulation of void growth for various line lengths, current densities or temperatures does not cover all the reported failure cases with a unique set of equations. However, the simulated stress distribution and the Blech effect successfully match experimental observations and are particularly useful for the optimization of circuit layout. In addition, it is possible to simulate various void shapes and the resulting electrical resistance to track critical failure modes. Finally, dispersion of measured parameters, such as MTF and post-mortem void size, is a strong limitation for model calibration but also an innovative field of investigation. Indeed, MTF spread is drastically reducing design margins and circuit robustness, therefore the simulation is suitable to explore the root cause of macroscopic dispersion.

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# 2

# Modeling electromigration using the peridynamics approach

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**Abstract**: This chapter presents a summary of the information and reasoning needed to justify learning about peridynamics for the purpose of analyzing electromigration and provides guidance for the development of a complete peridynamics analysis. The additions needed to convert the original peridynamics model as developed for mechanics problems to a multiphysics model capable of treating electromigration are reviewed. Experimental data on void drift by electromigration are introduced to provide a specific target for a demonstration of the peridynamical approach. Model results for the basic phenomena of this experiment are presented. The peridynamics approach appears capable of simultaneously accommodating both constitutive laws and explicit treatment of multibody interactions, for handling different aspects of the behavior of the material system to be modeled.

**Key words**: electromigration, interconnect, interface, modeling, peridynamics, theory, voids.

## 2.1 Introduction

### 2.1.1 Electromigration (EM)

Electromigration (EM) is a key reliability challenge for the economically very important electronics industry. EM in copper damascene interconnect structures is an extremely complex phenomenon because of the multitude of possible diffusion paths, including surfaces, grain boundaries, other internal interfaces, and 'bulk' material, and the multitude of driving forces for diffusion, which include gradients in atom or vacancy concentration, temperature, stress, and electrical current density, as well as the basic driving force of current density itself (Tan and Roy, 2007). Modeling EM with quantitative detail is an important aid in tracing physical EM phenomena back to their root causes, so that the damaging effects of EM, illustrated in Fig. 2.1, can be minimized in practical devices.



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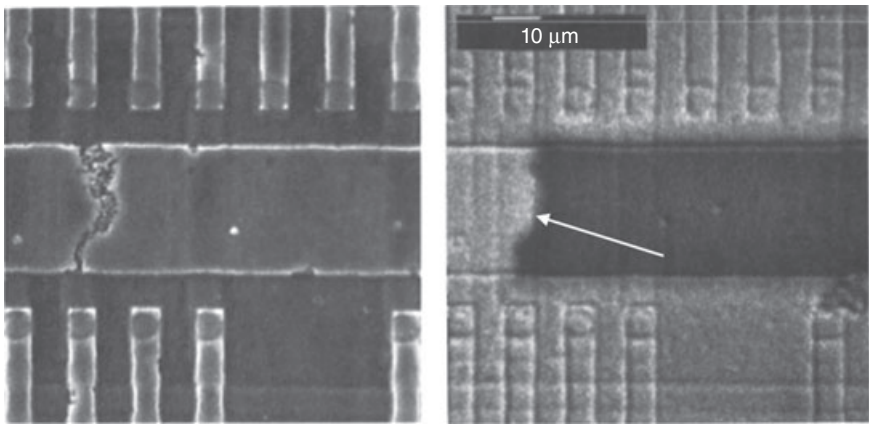


(a) (b)

*2.1* Scanning electron micrographs of the open circuit induced by EM in an n-MOS LSI (metal-oxide semiconductor for large-scale integration) bias metallization: (a) normal topographic image; (b) voltage contrast image. From Scorzoni *et al.* (1991). The contrast shown in (b) between the left and right portions of the wide conductor in the center of the image (white arrow) shows that the line is electrically discontinuous, and also shows that the location of the discontinuity coincides with the visible damage to the line.

### 2.1.2 Motivation for applying peridynamics (PD) to EM

Because practical failure mechanisms arising from EM include the nucleation, growth, motion, and agglomeration of voids, material discontinuities must be treated in a robust and efficient manner in any complete model of EM. The recently developed peridynamics (PD) approach to solid modeling has the key strength that its intrinsic nonlocal approach is tolerant of material discontinuities. Moreover, some of the key successes of the PD approach have been the realistic predictions of crack initiation and propagation in dynamic fracture experiments (Askari *et al.*, 2008).

### 2.1.3 Applicability of PD to EM

The application of PD to heat transport in solid bodies was suggested by Silling and Lehoucq (2008). We previously suggested the use of PD for simulating EM (Gerstle *et al.*, 2008, referred to here as PD-EM1) and gave details of the treatment within PD of the four important physical processes involved in EM, which are electrical conduction, thermal conduction, deformation and stress, and diffusion. The importance of these different mechanisms in EM led us to describe the PD approach to EM as a multiphysics model.

### 2.1.4 Scope

The first part of this chapter summarizes the detailed discussion given in PD-EM1. The latter part reports the computational implementation of a multiphysics PD model for EM along the lines previously proposed. This implementation was created as an extension of a publicly available PD code that was developed as part of a more general molecular dynamics (MD) code (lammps.sandia.gov). Finally, we present computational results for drift of a void impelled by EM, and point out certain correspondences between the model results and recent experimental observations. We suggest that this result is evidence of at least the possibility that modeling EM by use of a PD approach will prove useful.

## 2.2 Previous approaches to modeling electromigration (EM)

Each of the standard modeling approaches to EM has its obstacles. The PD-EM approach also has its own obstacles, which are explored in the context of the computational model discussed in the latter part of this chapter. Here we summarize the key obstacles for each of the standard approaches: MD; classical continuum analysis; and finite element analysis.

### 2.2.1 Molecular dynamics (MD) and EM

MD has been applied to EM by, for example, Bachlechner *et al.* (2005) and Chen *et al.* (2007). But such simulations, even on today's massive parallel computers, are limited to model sizes of perhaps ten million atoms for perhaps 100 ps. Thus, it remains true that the time/size scale accessible to MD is insufficient to model even a single crystallite, much less entire interconnect lines in integrated circuits.

### 2.2.2 Classical continuum modeling and EM

Classical continuum mechanical models have also been employed for EM (Maroudas and Gungor, 2002; Kim and Lu, 2006). Classical continuum mechanics is, however, not efficacious for analysis of fields that are, or may become, manifestly discontinuous, as shown for example in Fig. 2.1. Silling (2000) and subsequent publications have discussed the mismatch between the classical, field-based treatment of solid mechanics and several present-day problems that involve interfaces. Analogous arguments clearly apply to field-based treatments of the other physical phenomena involved in EM, namely, electricity, heat, and diffusion.

On a more philosophical level, because continuum mechanics allows singular solutions (for example, in stress and strain at the tip of a crack),

continuum mechanics is not a complete physical theory of solids, because such singularities are clearly non-physical. To remedy the situation, entirely new fields (fracture mechanics; nonlocal damage mechanics) have been developed over the course of the last century to augment continuum mechanics. PD has the favorable attribute that if the PD kernel is well-behaved, the theory does not allow singularities. Thus, PD is a complete theory that does not require auxiliary theories, such as fracture mechanics. This significantly simplifies computational implementation and ease of interpretation.

### 2.2.3 Finite element modeling and EM

Finite element analysis has been applied to EM in many studies, such as that by Tan *et al.* (2007). Indeed, the geometrical adaptability of the finite element approach is a key advantage. But finite element analysis requires a mesh; typically the meshes are matched to the solid surfaces, making applicability to moving voids difficult. The finite element treatment of fracture, taken as a representative example of problems with changing interfaces, is typically carried out by remeshing as the crack grows. Mesh dependences of both the initiation site of the crack and the path it takes are difficult to avoid. At a more fundamental level, the finite element approach is based upon the classical field equations, meaning explicit boundary conditions are needed at all boundaries.

### 2.2.4 Reasons for attempting a PD model of EM

The various approaches to modeling EM are described in more detail elsewhere in this book. Additional information can be found in PD-EM1. However, most of the previous efforts have focused on specific aspects of the problem, and therefore have an intrinsically limited regime of applicability, so they lack predictive capability for different cases. Our goal here as well as in PD-EM1 remains to significantly broaden the regime of applicability and to simplify multiphysical modeling of integrated circuits, by developing a modeling paradigm that can accurately and usefully predict the physical behavior of interconnects using today's computational capabilities. We choose, as reported in PD-EM1, to model EM using ideas from the PD model (Silling, 1998; 2000; 2002; Silling *et al.*, 2007). In contrast to classical continuum models, this model has several advantages, the foremost being that the response functions need not be continuous or differentiable. In addition, PD is a potential technique for multiscale modeling since it can relate the processes at the atomistic level to observable macroscopic quantities (Shen and Atluri, 2004; Tewary and Read, 2004; Read and Tewary, 2007) More details on the attractive features of the PD approach to EM modeling can be found in PD-EM1.

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## 2.3 Peridynamics (PD)

### 2.3.1 PD: mathematical basics

The PD approach to solid mechanics has been described in abundant detail in several publications including PD-EM1. The PD model starts with the assumption that Newton's second law holds true on every infinitesimally small differential volume within the domain of analysis. A force density function, called the pairwise force function (or PD kernel) $f$ (with units of force per unit volume per unit volume) between each pair of infinitesimally small differentiable volumes is postulated to act if the particles are closer together than some finite distance, called the material horizon, $\delta$. The pairwise force function may be assumed to be a function of the relative position and the relative displacement between the two particles, as indicated in Fig. 2.2. A spatial integration process is employed to determine the total force acting upon each differential volume, and a time integration process is employed to track the positions of the particles owing to the applied body forces and applied displacements. One of the advantages of the PD approach is that no finite element meshes are required. It is a meshless method. As described by Silling (1998 and subsequent publications), the PD model may be implemented on the computer as an array of interacting discrete particles or elements in a three-dimensional (3D) geometrical space. Computational implementations of PD models utilize elements of a size appropriate to the problem at hand.

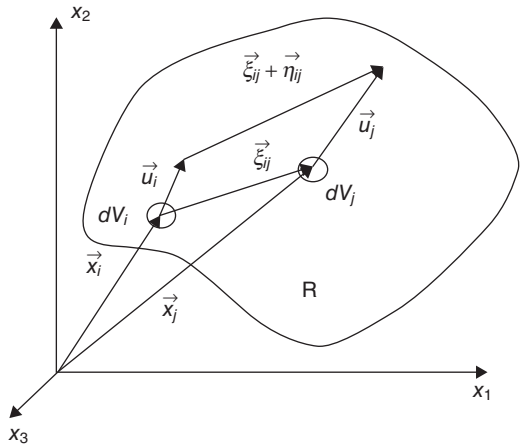
The description of the inter-element forces is phenomenological, like the elastic constants of solid mechanics, rather than an attempt to capture the complexity of atomic bonding. Unlike an MD model, a PD model has constitutive equations. However, unlike a finite element model, a PD model does not require continuous response fields. Silling and Lehoucq (2008) have given an extremely detailed treatment of how the interelement forces in PD describe the same physical behavior as the classical stress tensor field. Silling (2000) noted that the PD approach allows a reference position of the elements to be retained and used, in contrast to the MD approach.

Using the terminology given in Fig. 2.2, we assume that Newton's second law holds true on an infinitesimally small particle $dV_\mathrm{i}$ of mass $dm$, undeformed position $\vec{x}_\mathrm{i}$, and displacement, $\vec{u}_\mathrm{i}$, located within domain $R$:

$$dm\ddot{\vec{u}}_\mathrm{i} = \sum d\vec{F}_\mathrm{i}, \qquad [2.1]$$

where $\sum d\vec{F}$ is the force vector acting on the free body, and $\ddot{\vec{u}}_\mathrm{i}$ is particle $i$'s acceleration.

Dividing both sides of equation [2.1] by the differential volume of particle $i$, $\mathrm{d}V_\mathrm{i}$, and partitioning the force into components internal and external to the system of particles under consideration gives




*2.2* Interaction between differential volumes, as used in PD.

$$\rho\ddot{\vec{u}} = \vec{L} + \vec{b}, \qquad [2.2]$$

where $\rho$ is the mass density at position $\vec{x}_i$, $\vec{L}$ is the force vector per unit volume acting upon $dV_i$ owing to interaction with all other particles (for example, particle $j$) in domain $R$, and $\vec{b}$ is the externally applied body force vector per unit volume at position $\vec{x}_i$.

The internal material force density per unit volume $\vec{L}$ acting upon particle $i$ is an integral over all other particles $j$ within the domain $R$:

$$\vec{L} = \int_R \left(\vec{f}_{ij}\right) dV_j \qquad [2.3]$$

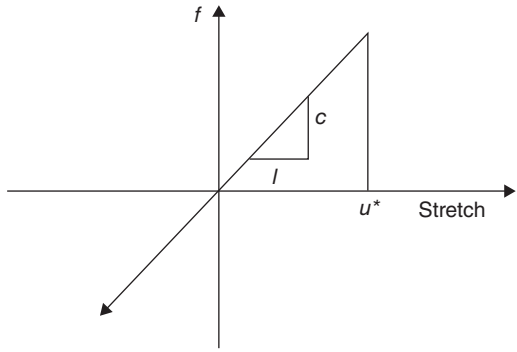
where $\vec{f}_{ij}$ is the PD force between $dV_i$ and $dV_j$. The pairwise force function, $\vec{f}_{ij}$ which has units of force per unit volume squared, can be viewed as a material constitutive property. In the simplest case, let us assume elastic behavior:

$$\vec{f}_{ij} = \vec{f}_{ij}\left(\vec{u}_j - \vec{u}_i, \vec{x}_j - \vec{x}_i\right) = \vec{f}_{ij}\left(\vec{\eta}_{ij}, \vec{\xi}_{ij}\right) \qquad [2.4]$$

where the pairwise force function is a function of relative displacement $\vec{\eta}_{ij}$ and relative position $\vec{\xi}_{ij}$ between particles $i$ and $j$. More complex constitutive relations, incorporating internal material state variables (such as damage), may also be contemplated.

Silling (1998) proposed a simple nonlocal PD constitutive model:

$$\vec{f}_{ij}\left(\vec{\eta}_{ij}, \vec{\xi}_{ij}\right) = c\left[\frac{\left(\left|\vec{\xi}_{ij} + \vec{\eta}_{ij}\right| - \left|\vec{\xi}_{ij}\right|\right)}{\left|\vec{\xi}_{ij} + \vec{\eta}_{ij}\right|}\right]\left[\frac{\left(\vec{\xi}_{ij} + \vec{\eta}_{ij}\right)}{\left|\vec{\xi}_{ij} + \vec{\eta}_{ij}\right|}\right] = cs\hat{u} \qquad [2.5]$$




*2.3* Microelastic PD model for quasibrittle material. This model governs the forces between two particles situated within the material horizon $\delta$ of each other.

if $\left(\left|\vec{\xi}_{ij}+\vec{\eta}_{ij}\right|-\left|\vec{\xi}_{ij}\right|\right)<u^*$ and $\left|\vec{\xi}_{ij}+\vec{\eta}_{ij}\right|<\delta$
Otherwise: $\vec{f}_{ij}\left(\vec{\eta}_{ij},\vec{\xi}_{ij}\right)=0$

where $c$, $\delta$, and $u^*$ are positive 'microelastic' constants, $s$ is the stretch of the bond, and $\hat{u}$ is a unit vector directed from particle $i$ to particle $j$. Thus, the 'spring' connecting any two particles is linear for small relative displacements, but it breaks when the relative displacement between the two particles exceeds $u^*$. Only particles within a distance from each other $\delta$ (the material horizon) in the deformed configuration interact. A simple microelastic PD model (with tensile limit) for brittle materials is shown in Fig. 2.3.

The PD model does not specify how the base-space (the particles) nor how the solution fields (such as displacements and temperatures) are to be represented. In most implementations to date, the particles are represented as finite-mass/volume discrete particles. Gerstle *et al.* (2007) represented the PD base-space using finite elements that may or may not be connected at the nodes. Fourier series or other wavelet-type functions to represent both the base-space and the solution fields can also be contemplated.

In a multiphysics setting, the constitutive model is expanded to account for thermal, electrical and diffusive effects. Each PD bond is generalized to become a conduction path for electrical current, heat transport, and mass transport. In PD-EM1 we gave the generalized constitutive laws listed in Table 2.1.

### 2.3.2 PD as applied: comparison and contrast with MD

A grossly oversimplified functional description would be that PD is a coarse-grained generalization of classical MD. MD analysis is described by

*Table 2.1* Multiphysics fields and equations for PD

| | Solid mechanics | Heat conduction | Electrical conduction | Atomic diffusion |
|---|---|---|---|---|
| Primary field | Displacement $\vec{u}$ | Temperature $T$ | Electrical potential $\Phi$ | Atomic concentration $C$ |
| Peridynamic flux | PD force $\vec{f}_F$ | PD heat flux $f_q$ | PD current flux $f_j$ | PD atomic flux $f_J$ |
| Constitutive relation | $\vec{f}_F = \vec{f}_F\left(\vec{\xi}, \vec{\eta}, \ldots\right)$ | $f_q = f_q\left(\vec{\xi}, \tau, \ldots\right)$ | $f_j = f_j\left(\vec{\xi}, \phi, \ldots\right)$ | $f_J = f_J\left(\vec{\xi}, \chi, \ldots\right)$ |
| Conservation equation | $\int_{H_F} \vec{f}_F dV_j + \vec{b} = \rho\ddot{\vec{u}}$ | $\int_{H_q} f_q dV_j + \bar{Q} = c_T \rho \dot{T}$ | $\int_{H_j} f_j dV_j + \bar{J} = c_E \dot{\Phi}$ | $\int_{H_J} f_J dV_j + \bar{K} = c_D \dot{C}$ |

Definition of symbols: $\vec{u}$ displacement; $T$ temperature; $\Phi$ electrical potential; $C$ atomic concentration (number of atoms per total number of initial lattice sites, equal to one minus the vacancy concentration); $\vec{f}_F$ peridynamic force per unit volume squared; $f_q$ peridynamic heat flow per unit volume squared; $f_j$ peridynamic current flow per unit volume squared; $f_J$ peridynamic concentration flow per unit volume squared; $H_F$, $H_q$, $H_j$, $H_J$ peridynamic neighborhoods of various fluxes for point $i$; $\vec{\xi}$ relative position in reference configuration of particle $j$ relative to particle $i$, $\vec{x}_j - \vec{x}_i$; $\vec{\eta}$ difference in displacement between points $i$ and $j$, $\vec{u}_j - \vec{u}_i$; $\tau$ difference in temperature between points $i$ and $j$, $T_j - T_i$; $\phi$ difference in electric potential between points $i$ and $j$, $\Phi_j - \Phi_i$; $\chi$ difference in atomic concentration between points $i$ and $j$, $C_j - C_i$; $\vec{b}$ applied body force per unit volume; $\rho$ mass density; $\ddot{\vec{u}}$ acceleration of particle i; $\bar{Q}$ applied heat flux (analogous to body force); $c_T$ heat capacity per unit mass; $c_E$ electrical capacitance (electrical charge per unit electrical potential per unit volume); $\bar{J}$ applied current flux (analogous to body force); $\bar{K}$ applied atomic concentration flux (atoms per unit time per unit volume, analogous to body force); $c_D$ atomic concentration capacity (atoms per unit concentration change per reference volume).

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Rapaport (1995). In an MD simulation, mathematical constructs representing atoms interact through interatomic potential functions that are designed to mimic actual interatomic forces in solids. Uniform strains can be applied by deforming the mathematical box containing the MD atoms; this allows the evaluation of the elastic constants predicted by the MD model. Special configurations such as surfaces and grain boundaries can be modeled. Forces from electrical charges on the atoms in MD, if present, are considered separately from the short-range interatomic forces. Such forces greatly complicate the MD computation, because of their long range. A computational PD model would implement these same capabilities.

Although MD models are structureless, meaning that the atoms of MD have no reference position, but rather can move freely in response to the sum of the forces from their neighbor atoms, PD models can accommodate numerical storage of states of several types, for example, the accumulated damage in each PD bond between particles. PD also makes use of constitutive laws, as indicated in Table 2.1, whereas in MD these laws are emergent from the behavior of the individual atoms. It is this use of constitutive laws that allows PD models to use time steps that are much longer than the femtosecond steps needed in MD.

## 2.4 PD and EM

### 2.4.1 EM master equation

EM is described by the drift equation, equation [2.6]. This is an Einstein–Nernst diffusion equation. However, certain terms in this equation represent complex material behavior rather than specific material properties.

$$v_{\mathrm{d}} = \frac{D_{\mathrm{eff}}(T)}{k\,T}\left(Z^{*}_{\mathrm{eff}} e \rho j - \frac{\partial \tau}{\partial x}\Omega\right) \qquad [2.6]$$

where $v_d$ is the drift velocity of the migrating atoms; $D_{\mathrm{eff}}$ is the effective diffusion coefficient; for the case where only a single diffusion mechanism is effective, $D_{\mathrm{eff}} = D_0 \exp(-E_{\mathrm{a}}/kT)$; $D_0$ is an experimentally determined constant (units: $m^2\ s^{-1}$). See for example Butrymowicz *et al.* (1973); $E_{\mathrm{a}}$ is the activation energy for diffusion. For bulk diffusion near room temperature, this includes the energy to create a vacancy at an atomic position in the crystal lattice plus the energy required to excite the vacancy to the saddle point between two atomic positions; $k$ is the Boltzmann constant; $T$ is the absolute temperature; $Z^{*}_{\mathrm{eff}}$ is the effective charge of the atoms. It represents the strength of the interaction of the 'electron wind' with the atoms, as a multiplier of the electrostatic interaction between a charged atom and the applied electric field that is producing the current; $e$ is the fundamental charge; $\rho$ is the resistivity; $j$ is the current density (A $m^{-2}$);

$\partial\tau/\partial x$ is the partial derivative of stress with respect to position; and $\Omega$ is the atomic volume.

Equation [2.6] lists only two driving forces for EM, namely, the electric current and the stress gradient. Others are possible, foremost among them being temperature gradients and gradients in the concentration of atoms or vacancies (Tan and Roy, 2007). Equation [2.6] includes only one diffusion path, but, in reality, EM results from multiple pathways including surface, interface, grain boundary, pipe, and lattice diffusion (Ogawa *et al.* 2002; Tan and Roy, 2007).

Ogawa *et al.* (2002) indicate that the various pathways for EM damage formation can be examined using the first term on the right-hand side of equation [2.6]. The various pathways can be expressed as:

$$Z^*_{\text{eff}}D_{\text{eff}} = Z^*_{\text{B}}D_{\text{B}}F_{\text{B}} + Z^*_{\text{S}}D_{\text{S}}F_{\text{S}} + Z^*_{\text{I}}D_{\text{I}}F_{\text{I}} + Z^*_{\text{GB}}D_{\text{GB}}F_{\text{GB}} + Z^*_{\text{P}}D_{\text{P}}F_{\text{P}} \quad [2.7]$$

Equation [2.7] illustrates the analysis of the product of the effective charge number and the effective diffusivity into its component parts. The subscripts identify pathways of diffusion by

- $B \equiv$ bulk,
- $S \equiv$ surface (if it exists),
- $I \equiv$ interface (if it exists, in the particular interconnect),
- $GB \equiv$ grain-boundary, and
- $P \equiv$ pipe, meaning, through dislocation cores.

$F_j (j = B, S, I, G, P)$ is the fraction of atoms diffusing through a given pathway, which depends on the material and the specimen geometry, and probably on other quantities such as the temperature as well. Ogawa *et al.* (2002) explain that each pathway is anticipated to have a different $Z^*$ component because the wind-force varies according to the local electronic environment surrounding a given atom (Sorbello, 1996).

## 2.4.2 Assumptions for modeling EM by PD

The importance of interfaces in the modeling of EM has already been emphasized. A second important and challenging aspect of EM is that the diffusion pathways can be modified during EM. For example, a void can grow, changing the area available for surface diffusion. An important consideration in the modeling of EM is the capacity of a modeling approach to handle these changes. Our interest in PD as a modeling approach for EM stems from our opinion that PD offers a more workable treatment of these key features of the EM problem. We believe that PD is 'scalable', so that the different diffusion paths and driving forces can be treated with a controllable degree of effort according to the goal of the modeling.

Equation [2.6] shows how the electric current, the temperature, and the stress enter into the EM problem. A key issue for the application of PD to EM is whether PD's nonlocal approach to solid-state phenomena is applicable to electric charges and fields, heat transport, and diffusion. In PD-EM1 we gave a detailed statement of a set of equations for fields, fluxes, constitutive relations, and conservation rules developed by analogy between solid mechanics and these various physical phenomena. Here, as in PD-EM1, we simply assume that because the field equations for electricity, heat, and diffusion are similar to those for deformation, and because the PD approach is mathematically consistent with the field equations for deformation (Silling and Lehoucq, 2008), then the PD approach is also consistent with the field equations for electricity, heat transport, and diffusion. The treatment of these different physical phenomena within PD probably involves mathematical restrictions; here we simply assume that these are not prohibitive.

### 2.4.3 Mathematical specifics for EM by PD

The problem of long-range electrical interactions is not addressed in the PD model used here. The PD elements are uncharged, so they feel no electrostatic forces. To treat the electrical currents that drive EM, the model includes charge transport among elements, according to the usual relation

$$\mathbf{J} = \sigma\mathbf{E} \qquad [2.8]$$

where $\mathbf{J}$ is the electric current density, $\mathbf{E}$ is the electric field vector, and $\sigma$ is the electrical conductivity. The electric field is notionally given by the standard relation from electricity theory:

$$\mathbf{E} = -\mathbf{grad}\ V \qquad [2.9]$$

In the PD model we use:

$$E_{ij} = \frac{(V_j - V_i)}{(r_j - r_i)} \qquad [2.10]$$

for calculating charge transport from element $i$ to element $j$. We take $V_i$, the potential on element $i$, as simply proportional to the charge on element $i$. This approximation, in particular, clearly requires further study. The result is

$$J_{ij} = \sigma_{ij}\frac{(V_j - V_i)}{(r_j - r_i)} \qquad [2.11]$$

where the conductivity $\sigma_{ij}$ can be chosen based on the properties of the PD elements $i$ and $j$.

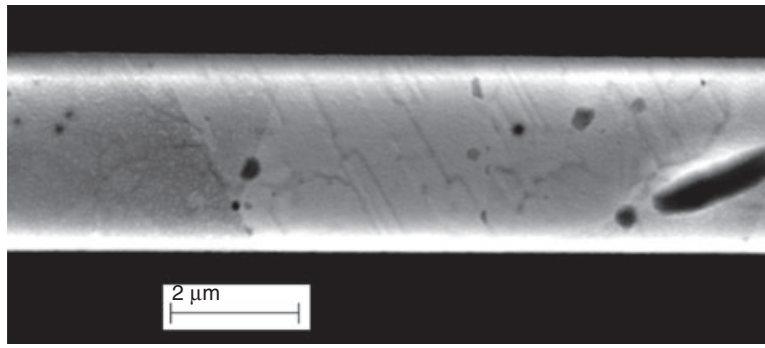
As in PD-EM1, the conduction of heat and the diffusion of atom concentration are handled similarly, with temperature and atom concentration analogous to voltage and heat and number of atoms analogous to charge in the relations above. In PD-EM1 we showed that a one-dimensional PD model of a conductor reproduced the classical linear distribution of electrical potential and the parabolic distribution of temperature for a wire heated by Joule heating with no loss of heat at the lateral boundaries. Here, again, we show that a 3-dimensional PD approach reproduces the same simple classical solutions to the model problem.

## 2.5 Illustrative example

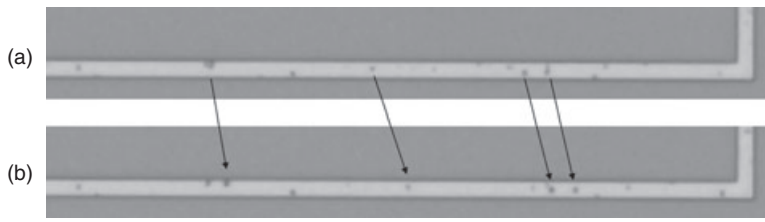
### 2.5.1 Problem to be modeled

Of the many reports in the literature on observations of EM in electronic interconnects, the vast majority focus on either voiding or voids. Voiding refers to the complete disappearance of a certain segment of the length of a conductor, whereas voids are cavities or holes in a conductor. Here we focus on the motion of a single void in a conductor enclosed in dielectric. We note in passing that other aspects of void behavior, such as the evolution of void shape, have been both observed and modeled. We also note that the nucleation of voids is a critical issue in the reliability of microelectronic interconnects, although here we take a void as given. The objective of this section is to identify a particular observed instance of an EM phenomenon, and construct a preliminary PD model of this experimental situation. Here we are only attempting to show the plausibility of modeling this situation by PD. It becomes evident from this example that constitutive laws have a key role in PD modeling.

The motion of a void in a current-carrying conductor was examined by Ho (1970); the approach was continuum mechanics. Few observations of the situation modeled by Ho have been carried out. We have obtained experimental data on a similar system. The main difference is that whereas Ho predicted the speeds of spherical and cylindrical voids, we observed the motion of surface voids. We created voids in copper conductors by the application of high amplitude alternating current (ac) (Read *et al.*, 2009). The specimens were damascene copper lines with width 3 μm, thickness 0.5 μm, and length 200 μm, completely enclosed in $SiO_2$ dielectric. A typical scanning electron microscopy (SEM) micrograph, taken after stressing a line with ac and later removing the dielectric on top of the copper, is shown in Fig. 2.4. The voids appear as round dark regions in the conductor. The void depth is not measurable from the plan-view SEM images. Because we have detected the presence of copper in the center of these voided regions by use of energy dispersive X-ray spectroscopy (EDS), we believe they




*2.4* SEM micrograph showing typical appearance of a wide copper damascene line constrained in $SiO_2$ after ac stress. The peak current density was 14.4 A $cm^{-2}$. The lifetime was 1498 s. The peak temperature rise, from Joule heating, was 396°C .




*2.5* Enhanced optical images of a line of the same type as shown in the previous figure: (a) voids (dark spots) in fully contained copper damascene line; (b) same line after dc stress, showing that some of the voids have moved by electromigration. Eight additional intermediate images acquired during the experiment, not shown, allowed unambiguous identification of the moving voids.

penetrate only part-way through the thickness. The particular experiment of interest here was performed on a different line, with the dielectric cap still present. After the line was stressed with ac, several voids were visible optically on the top surface, as shown in Fig. 2.5a.

Because this image has been enhanced to increase the contrast between the voids (dark spots) and the copper (lighter strip), the dark spots reveal only the presence and locations of the voids, but do not portray their shapes accurately.

When we applied a direct voltage and current (dc), the voids moved steadily under the effect of the current, and their changing positions were captured by optical imaging. Over the course of the experiment about 100 images were obtained. Figure 2.5a shows the first and Fig. 2.5b shows the tenth. Each void was sufficiently far from the others that its behavior was

independent of the other voids. The fastest-moving voids moved at a similar rate of approximately 0.08 μm $s^{-1}$ for the particular experimental conditions, approximate current density 15 MA $cm^{-2}$ and temperature 380 °C. Other voids moved more slowly, and still others at varying rates.

## 2.5.2 Implementation of PD model

A hypothetical copper conductor with a total length of 310 nm and a width and height of 90 nm was modeled as a rectangular parallelepiped of 2511 PD elements, of which 324 were in boundary regions and 2187 were fully active elements. Each PD element represents a cube 10 nm on each side. A constant voltage was applied between the end boundary regions of the conductor. The sides of the conductor were treated as adiabatic, while the ends were maintained at a fixed temperature. As noted in previous chapters, the surface diffusion rate of copper is known to be much greater than the bulk diffusion rate. For this reason the surfaces of copper conductors in practical interconnects are coated with barrier layers that prevent surface diffusion. Therefore, the lateral surfaces of the model conductor were assigned diffusion rates equal to the bulk rate. A surface void was modeled by assigning an initial atomic concentration of 0.99 to a $3 \times 3$ block of nine adjacent elements on the surface of the conductor.

The PD elements of the model were visualized as blocks containing variable electric charge, temperature, and atomic concentration. In this initial demonstration, the PD elements were not allowed to move. The physical justification for this was that actual interconnect conductors are fixed in a rigid framework of dielectric supported by a silicon slab, and so are highly constrained mechanically. The transport of atomic concentration between blocks was treated under the framework listed in Table 2.1. The master equation for EM given in equation [2.6], was applied to calculate the amount of atomic concentration transported at each time step between each pair of interacting elements. The formula used was that the fraction of atomic concentration d$C$ transported through each PD bond during a single time step d$t$ was:

$$dC = dtv/l \qquad [2.12]$$

where $v$ is the drift velocity from equation [2.6] and $l$ is the size of an element, in this case, 10 nm. The units in equation [2.12] are consistent because the atomic concentration $C$ is dimensionless. In the present calculation, the stress gradient term on the right hand side of equation [2.6] was not considered. Stresses in a more detailed model could be calculated from the inter-element forces given by equation [2.5]. These forces could also be used to displace the elements, but this was not done here as discussed above. The current density in the PD model was calculated within the framework

listed in Table 2.1 by allowing electrical charge to flow between neighboring elements according to equations [2.8]–[2.11]. This charge was used to establish the voltage on each PD element, beginning with the usual formula that relates the geometry of a conductor to its resistivity:

$$R = \rho L/A \qquad [2.13]$$

where $R$ is the electrical resistance, $\rho$ is the electrical resistivity, $L$ is the length of the conductor, and $A$ is the cross-sectional area. In the present model, the length $L$ was taken as the element size, 10 nm; if the area $A$ had been taken as the block area, here 100 $nm^2$, an incorrect value of the electrical resistance of the modeled copper conductor as a whole would have resulted. The reason for this is that charge is transported through the PD model conductor through each PD bond between neighboring elements; this produces an effective area different from the simple geometrical value of 100 $nm^2$. An 'effective area factor' was used to account for this effect. This factor is different for different values of the interaction horizon among the PD elements. In the present model with its simple cubic lattice of elements, each element is assumed to interact with its 26 nearest neighbors.

Below a calculated temperature distribution is presented, based on electrical fields and currents calculated using equations [2.8]–[2.11] and the relationship:

$$p = Ej \qquad [2.14]$$

where $p$ is power density and $j$ is current density. However, another simplification in the present calculation of void motion was that the temperature was assumed to be a constant independent of position. This was done to simulate the present experimental case, where the temperature over the region of the conductor that was traversed by the voids is constant. In practice an alternative form of equation [2.6] was formulated by replacing $j\rho$ with $E$ since by definition (for scalar conductivity, as is appropriate for copper):

$$\rho = 1/\sigma \qquad [2.15]$$

The physical sense of this substitution is that the interaction between the electron wind and the lattice ions is proportional to the electric field because, although the amount of current flowing increases with increasing conductivity, the interaction between the flowing electrons and the fixed ions increases in strength with increasing resistivity. The effects of conductivity and resistivity cancel, leaving the electric field term.

The constitutive parameters used in the present calculation are listed in Table 2.2. Customary units for each parameter are used.

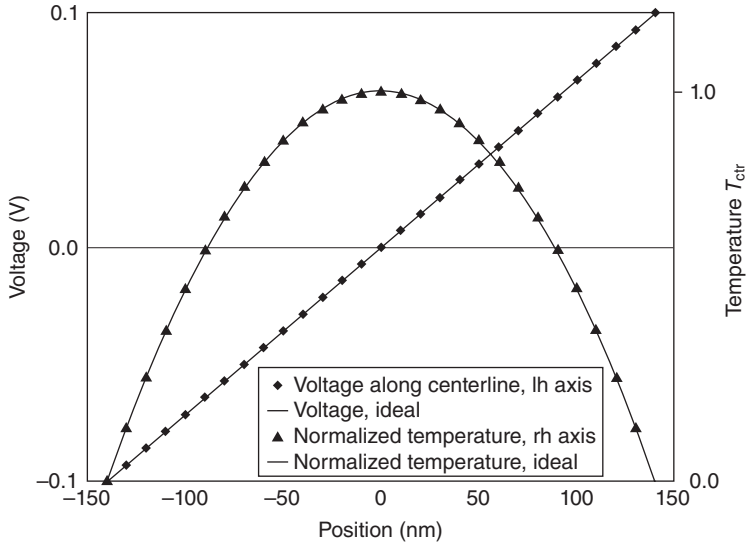
The numerical calculations for the new multiphysics PD model of EM were implemented through the use of a computer code for the PD model

*Table 2.2* Constitutive parameters and temperature used in calculations. Customary units for each parameter are used

| Parameter | Symbol | Value | Unit |
|---|---|---|---|
| Electrical conductivity | $\rho$ | 2.0 | $\mu\ \Omega$ cm |
| Bulk diffusion constant | $D_0$ | 0.625 | $cm^2\ s^{-1}$ |
| Surface diffusion constant | $D_s$ | 0.63 | $cm^2\ s^{-1}$ |
| Activation energy for bulk diffusion | $E_{a,b}$ | 2.10 | eV |
| Activation energy for surface diffusion | $E_{a,s}$ | 1.18 | eV |
| Heat capacity of copper | $C$ | 3.48 | $J\ cm^{-3}$ |
| Thermal conductivity of copper | $K$ | 401 | $W\ m^{-1}K^{-1}$ |
| Temperature (absolute) | $T$ | 600 | K |

of mechanics that has been made available by Sandia National Laboratories (lammps.sandia.gov). The organization of the source code facilitates modifications for new situations such as EM. Code was added to input the additional constants needed in the constitutive laws used here, such as electrical resistivity, thermal conductivity, heat capacity, and diffusion constants. Arrays for storage of the values of the additional physical quantities needed in this multiphysics version of PD, specifically, voltage, temperature, and atom concentration, were added to the code. Routines for the flow of electrical current, heat, and atom concentration were inserted. The new results, voltage, temperature, and atom concentration at each PD element, were listed by use of existing routines in the code. Graphical representations of the results were created using a companion set of software.

We introduced various timescales appropriate to the various physical quantities involved, which were electrical charge and potential, heat and temperature, and stress and deformation. It is apparent from the physics of this problem that the first event to be modeled is the establishment of electrical current through the conductor, and that this must occur rapidly compared with other events in the problem. We found that thousands of time steps were needed to stabilize the charge and potential distributions. These were iterated on the fastest model time scale. The temperature distribution was then stabilized based on an independent time scale. For this first attempt, we neglected the temperature dependence of the electrical conductivity. To treat variable thermal and electrical conductivities, the electrical and thermal quantities would have to be converged by iterating them repeatedly in turn. The transport of electrical charge, heat, and force between PD elements within the same 'horizon' were treated according to the prescriptions given in Table 2.1 as explained in PD-EM1. Figure 2.6 shows that the resulting voltage and temperature distributions converged to their ideal values, which were, respectively, linear and parabolic, for this simple situation. This convergence demonstration was calculated in the




*2.6* Voltage and temperature variation along the centerline of the modeled conductor as calculated iteratively by the PD approach, compared with their ideal values.

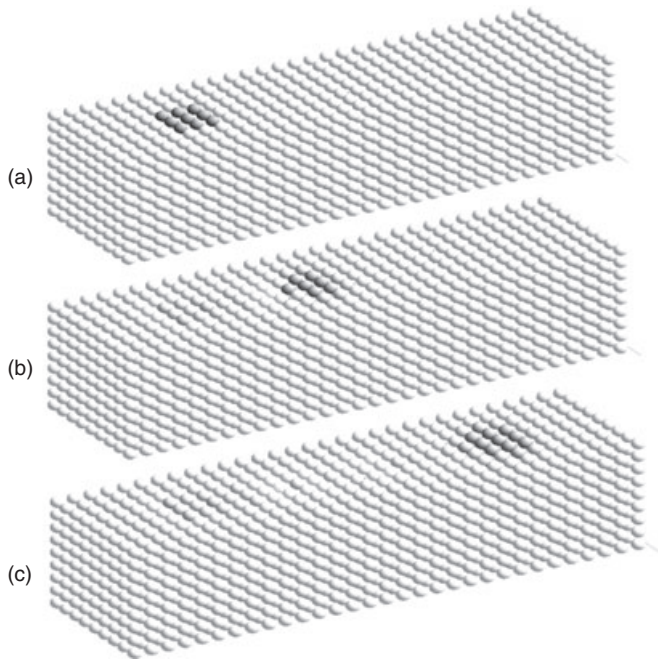
absence of a model void, to allow direct comparison to available ideal values. The data shown required 9816 iterations of the voltage calculation and 814 for the temperature calculation.

With current, temperature, and stress all stabilized, the diffusion steps were allowed to begin. Under these extremely oversimplified assumptions, the void gradually dissolved and dispersed through the conductor.

More realistic physical modeling assumptions were deduced by considering the physics of an actual surface void. A void has an internal surface; diffusion on this surface is responsible for the drift of the void under EM, as modeled by Ho (1970). Rapid diffusion on the void surface was introduced into the present model by assigning diffusion constants according to the local atom concentration. The surface diffusion rate, which is thousands of times faster than the bulk rate that corresponds to regions of normal atomic concentration, was assigned to regions of low concentration, considered as representing a void. For this case the void migrated steadily along the conductor, but it dissolved at the same time. This was inconsistent with the experimental observations. Most of the experimentally observed voids, especially those toward the cathode end of the line, appeared to be stable. They did not decrease in size or dissolve. Therefore to model this behavior, two correction terms were included. One was a 'surface energy' term that increased the diffusion rate when it would promote the increase of void concentration in one element by absorbing void fraction from a neighboring

element with a much smaller concentration. The idea is that for two equal volumes of voids, one volume composed of many small voids and the other composed of a single larger void, the multiple smaller voids have a total surface energy larger than the single larger void. The thermodynamics should therefore favor the growth of the larger void, because this lowers the surface energy. The other correction tested was a 'stress energy' term that penalized the diffusion of atoms into regions where the atom concentration was 1 or larger.

Under these *ad hoc* constitutive laws, the initial void grew in size as it migrated along the line, but it retained its visibility and reached the other end of the line. Initial, intermediate, and final state images are shown in Fig. 2.7 a–c. The small spheres in the graphic represent PD elements. Darker areas indicate reduced atomic concentrations, which is the numerical representation of a void in this model. Figure 2.7 represents a calculation where a 1% reduction in atomic concentration corresponds to the model void. For this case, the criterion for application of the surface diffusion rate was an atomic concentration below 0.996. Because each PD element in the model




*2.7* PD model calculation results showing (a) initial, (b) intermediate, and (c) final stages of PD calculation of void motion. The darker areas indicate reduced atomic concentrations, which is the numerical representation of a void in this model.

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represents 1000 $nm^3$, a literal interpretation of this calculation would be that the initial void had a volume of 10 $nm^3$ for each of the dark-colored elements in the figure, for a total of 90 $nm^3$. Its velocity was about 453 nm $s^{-1}$. A similar calculation was carried out for an initial assumption of a 10% reduction in the atomic concentration within the void region. In this case, the criterion for the use of the surface diffusion rate had to be adjusted to an atomic concentration of 0.96, and a slight adjustment in the surface energy improved the stability of the void. This larger model void traveled more slowly by almost a factor of 10. This is generally consistent with Ho's (1970) result, which had the void speed inversely proportional to the radius (larger voids drift more slowly).

The run time on a single-processor desktop computer was 203 s. Most of this time was required to converge the charge and temperature distributions. The run included 750 diffusion time steps.

## 2.6 Computational requirements: present and future

The computational effort involved in PD modeling a problem involving a number $N$ of PD elements is roughly similar to that in involved in a MD model of $N$ atoms. Although the PD force law described in equation [2.5] is simpler than many interatomic force laws, the addition of additional types of physics in a multiphysics PD model consumes additional computational effort. Gerstle *et al.* (2010) reported the computational effort involved in the use of PD to model the failure of a concrete joint. It was found that, by use of today's massively parallel computer systems, it is possible to model 3D reinforced concrete components of significant size (such as parts of beams and columns, and connections) using the PD model. However, modeling entire buildings or bridges using PD is not currently feasible.

Simulation of EM problems is somewhat more computationally intensive because of the more complex types of physics involved. However, it appears that simulation of million-particle EM problems are well within the reach of present high-performance computing systems.

### 2.6.1 Green's function method for improving the computational efficiency of the PD model of EM

As is apparent in the preceding sections, the PD model involves solution of a many-body problem of $N$ interacting discrete elements. As such, it is closely analogous to an $N$-atom problem in solid-state physics. Powerful computationally efficient techniques have been established for solution of such problems. These techniques can be, in principle, incorporated into the PD model. One such technique is the lattice Green's function method for static as well as time dependent problems. The lattice static Green's function

method (Tewary, 1973) has been successfully used for modeling defects in crystal lattices. A hybrid technique based upon the use of both MD and Green's functions has also been developed (Tewary and Read, 2004; Read and Tewary, 2007) and applied for multiscale modeling of nanomaterials. For time dependent problems, the causal Green's function method has been shown to extend the time scales by several orders of magnitude (Tewary, 2009). In this section, we briefly review these techniques and indicate their possible application to PD problems.

In the example given in 2.5, we made several simplifying assumptions in order to illustrate the application of the PD model to EM without clouding it with mathematical details. A fully-fledged three-dimensional calculation, which has not yet been carried out for EM using the PD model, consists of solving equation [2.2] for relative displacements that are time dependent. This equation can be solved by using the methods similar to MD. However, for realistic modeling, $N$ needs to be of the order $10^4$ or even larger. For large values of $N$, the solution of equation [2.2] becomes computationally very expensive. A major problem in MD is its extremely limited time scale. Most MD calculations are limited to 10–100 ps. For modeling many physical processes such as EM, it is necessary to model time up to a few micro-seconds or even more. For realistic values of $N$, this is a formidable task even for modern computers. We propose that it should be possible to address this problem by using the causal Green's function technique (Tewary, 2009). Here we outline the approach.

### 2.6.2 Mathematics for application of causal Green's function to PD

The PD force as defined by equation [2.4] must be an analytic function of the displacements. We can, therefore, expand it in a Taylor series in the displacements $u_j$ about the equilibrium sites of the elements, as follows:

$$f_{ij}(\eta_{ij}, \xi_{ij}) = f0_{ij} + \Phi_{ij}u_j + \Delta f_{ij}\Phi_{ij}(u_j) \qquad [2.16]$$

where $f0_{ij}$ is the constant term and $\Phi_{ij}(u_j)$ is the linear Taylor coefficient evaluated at the equilibrium values of $\xi_{ij.}$ The remaining term $\Delta f_{ij}\Phi_{ij}(u_j)$ represents the nonlinear contributions and contains quadratic and higher powers of $u_j$.

In equation [2.16], $\phi_{ij}$ can be identified as a $3\,N \times 3\,N$ matrix, and $f0_{ij}$, $u_j$ and $\Delta f_{ij}$ as $3\,N \times 1$ column matrices corresponding to $N$ PD elements. The factor 3 arises because each element has three degrees of freedom in the 3D Euclidian space. The integration over the volume element $dV_j$ and the functional dependence of $f_{ij}$ on position co-ordinates in equation [2.16] and subsequent equations are not explicitly shown for reasons of brevity.

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Note that $f_{ij}$ in equation [2.16] depends only upon the displacement of a single element $u_j$, whereas it depends upon the relative displacement $\eta_{ij} = u_j - u_i$ in equation [2.2]. This apparent inconsistency can be removed by defining the self PD force $f_{ii}$ using the following relation:

$$\Sigma_j f_{ij} = 0 \qquad [2.17]$$

where the sum includes $j = i$. This gives the following value for the self-peridynamical force:

$$f_{ii} = -\Sigma_j f_{ij} \cdots (j \neq i) \qquad [2.18]$$

The self force is not normally defined in the PD model.

Using equation [2.16], we can write equation [2.2] in the form

$$\mathbf{Mu} = \mathbf{b}^*(\mathbf{u}) \qquad [2.19]$$

where **M** is an operator defined by

$$\mathbf{M} = \rho\partial^2/\partial t^2 - \Phi \qquad [2.20]$$

and

$$\mathbf{b}^*(u) = f0 + b + \Delta f(u). \qquad [2.21]$$

Equation [2.19] is analogous to the Born von Karman equation for $N$ atoms in lattice dynamics (see, for example, Maradudin *et al.*, 1971), except for the nonlinear term $\Delta f(u)$ on the right in equation [2.21] for **b***. The Fourier transform of **M** is exactly the lattice dynamical matrix of the Born von Karman model and $\mathbf{\Phi}_{ij}$ corresponds to the force constant matrix connecting atoms $i$ and $j$. Equation [2.17] corresponds to the condition of invariance of the crystal energy against rigid body translation [Maradudin *et al.*, 1971] that yields the self force constant of each atom as in equation [2.18].

Equation [2.19] should therefore be amenable to the powerful computational techniques developed for the nonlinear Born von Karman model for static as well as time-dependent problems. The operator on the left of equation [2.19] is linear, so we can define the corresponding Green's function operator as follows:

$$\mathbf{G} = \mathbf{M}^{-1} \qquad [2.22]$$

This gives the following formal solution of equation [2.19] in the operator form:

$$\mathbf{u} = \mathbf{G}\mathbf{b}^*(\mathbf{u}) \qquad [2.23]$$

In the static case, the time derivative of **u** is zero and **G** becomes the static Green's function (Tewary, 1973). Equation [2.23] can then be used to calculate **u** for modeling cases when one (or a finite number) of the PD

elements is 'defective'. A defective element is defined as the element that is different from the other elements and has a different $f_{ij}$. It can represent a void or a hillock or some other defect in the solid. In such cases, we have to calculate the defect Green's function (Tewary, 1973). The effective force term $\mathbf{b}^*(\mathbf{u})$ can be identified as the Kanzaki force (Tewary, 1973; Tewary, 2004). Calculation of the Kanzaki force in the nonlinear case by using MD has been given by Read and Tewary (2007) for a quantum dot in silicon.

In the time dependent case, the inverse of $\mathbf{M}$ can be obtained by taking the Laplace transform of equation [2.22]. This gives:

$$\mathbf{G}\hat{}(\mathbf{s}) = [\rho s^2\mathbf{I} - \Phi]^{-1} \qquad [2.24]$$

where $\mathbf{I}$ is the $3N \times 3N$ unit matrix, $\mathbf{G}\hat{}(\mathbf{s})$ is the Laplace transform of the Green's function, and $s$ is the Laplace variable. Equation [2.24] shows that $\mathbf{G}\hat{}(\mathbf{s})$ has poles in the complex $s$ plane at the eigenvalues of $\Phi$. If $\Phi$ is positive definite, all the poles are on the real axis. The causal Green's function can be obtained analytically by taking the inverse Laplace transform of $\mathbf{G}\hat{}(\mathbf{s})$ by choosing a suitable contour in the $s$-plane (Tewary, 2009).

In the linear case when $\mathbf{b}^*(\mathbf{u}) = \mathbf{b}$, the causal Green's function yields an exact analytical solution of equation [2.23] for $\mathbf{u}$ that is valid at all times. In many cases of physical interest $\mathbf{u}$ may be small enough for the linear approximation to be valid. In EM and other similar problems involving large displacements of the elements, $\Delta\mathbf{f}$ is, in general, nonzero. In such cases equation [2.23] is solved numerically by using a step-by-step iterative technique in space (Tewary, 2009). At each step, $\mathbf{f}$ is expanded locally keeping only the linear terms in $\mathbf{u}$ as given by equation [2.16]. The integration over time is obtained exactly by taking the inverse Laplace transform of $\mathbf{G}\hat{}(\mathbf{s})$ (Tewary, 2009). Each step size is chosen to be small enough so that $\Delta\mathbf{f}(\mathbf{u})$ is negligible during that step. Because the force is recalculated at each step, the final solution includes the nonlinear effects as in conventional MD. However, neglecting $\Delta\mathbf{f}(\mathbf{u})$ at each step introduces a constraint on the time step, but it is much less severe than that in the conventional MD because (Tewary, 2009):

1. In the conventional MD, the force during each time step is approximated by $f0$ and both the linear term $\Phi$ and the nonlinear term $\Delta\mathbf{f}$ in equation [2.16] are neglected. In the GF method the linear term is also retained in addition to $\mathbf{f0}$. This gives a much better approximation of the variation of the force during the time step.
2. The time integration in the conventional MD is carried out numerically using the linear approximation. In more refined versions of the MD, quadratic terms in time are also included. In the GF method, the time integration is carried out analytically to give the exact result for each time step.

In general, the Green's function method requires inversion of a matrix. In symmetric cases, the matrix inversion is easily performed by using the discrete Fourier transform in space (Tewary, 1973; Tewary, 2004). In more general cases, the inversion can be done by iteration and is facilitated by the fact that $\Phi$ is a sparse matrix. The choice of method of calculating $\mathbf{G}$ would depend upon the specific physical problem.

More details on the static and causal Green's function methods and their application to the PD model for EM will be presented in a forthcoming paper. The other associated multiphysics PD problems such as distribution of electrical charge, current, and temperature, as for example in the solution of equation [2.8], can also be solved by using the Green's function approach. The Green's functions for these problems are well known (see, for example, the classic text by Morse and Feshbach, 1953). These techniques may be useful for modeling EM in complex and variable geometries.

## 2.7 Conclusions

The 'lessons learned' in this initial attempt to construct a multiphysics PD modeling approach to EM include:

1. The PD treatment of interaction among solid elements, which may be individual atoms or larger blocks, appears capable of handling the transport of electrical charge, heat and matter with physically sensible results for the elementary situations attempted.
2. It was necessary to use separate time scales for the transport of electrical charge, heat, and matter. The distributions of electrical potential and temperature were converged, using iterations as necessary, as a preliminary part of each full time step. The number of calculation steps required to reach convergence of the distribution of electrical potential was substantial. Only after this convergence was mass transport (diffusion) calculated at each time step.
3. The main contrast between the PD approach and the classical continuum approach is that PD naturally accommodates dynamic internal (and external) interfaces.
4. The main contrast between the PD approach and the MD approach is that PD accommodates constitutive laws for its transport properties. This allows treatment of slow processes, in particular, mass transport by diffusion.
5. The adaptation of constitutive laws for diffusion to the particular PD model at hand is an *ad hoc* process, which depends on the coarseness of the model both in time and in spatial extent. In this illustrative model of EM, a criterion for where to apply the surface diffusion rate and a surface energy function were applied.

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6. Continuing advances in the cost-effectiveness of computational power and in the power of mathematical formulations such as Green's functions provide assurance that available computational resources are sufficient for useful application of PD to various physical phenomena including EM.

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# 3

# Modeling, simulation, and X-ray microbeam studies of electromigration

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**Abstract**: Modeling and simulation coupled with X-ray microbeam studies, where local elastic strains are measured, can be used to resolve some of the challenging questions regarding the physics of electromigration. This chapter provides an introduction to the prevalent modeling methodology and three key issues that are currently unresolved: (i) how does the diffusing mass arrange itself and the effect of diffusion path, (ii) what is the appropriate driving stress, and (iii) determination of effective charge number $Z^*$. Analytic and finite element modeling formulations are presented and used with two X-ray microbeam data sets, exhibiting opposing trends, to demonstrate how these questions may be answered.

**Key words**: electromigration; Eshelby model; finite element model; X-ray microbeam; effective charge number.

## 3.1 Introduction

Models for predicting stress evolution during electromigration in metallic interconnect lines start with an equation for the atomic or vacancy flux, which, for the case of the atomic flux vector $\boldsymbol{J}$, typically has a form like (Korhonen *et al.* 1993):

$$\boldsymbol{J} = \frac{D}{\Omega k T}\left(-e\rho|Z^*|\,\boldsymbol{j} + \Omega\nabla\bar{\sigma}\right) \qquad [3.1]$$

where $D$ is an average mass transport diffusion coefficient, $k$ is the Boltzmann constant, $T$ is the absolute temperature, $\rho$ is the electrical resistivity, $e$ is the elementary charge, $Z^*$ is the effective charge number, $\boldsymbol{j}$ is the current density, $\Omega$ is the atomic volume, and $\bar{\sigma}$ is a stress (tensile taken as positive here). The stress in Eqn. [3.1] is taken as either the normal stress on a grain boundary (Blech and Herring 1976, Gleixner and Nix 1999, Korhonen *et al.* 1993, Povirk 1997) or the hydrostatic stress (Hau-Riege and Thompson 2000, Sarychev *et al.* 2000, Wang *et al.* 1998). The first term on the right hand side in the parentheses represents the atomic driving force



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associated with the electric current (the electromigration driving force), and the second term represents the mechanical driving force. A similar equation results when vacancy fluxes are considered, but in the opposing direction since the mass diffusion process is associated with the exchange of atoms and vacancies. The divergence of the atomic flux vector $\boldsymbol{J}$ is associated with the depletion (when the divergence is positive) or the accumulation (when the divergence is negative) of material at a point in the interconnect line. If the interconnect line is confined, the depletion or accumulation of material at any given location leads to a change in the stress state, which causes an increase in the mechanical driving force in equation [3.1] acting to oppose the electromigration induced mass flux. If the conductor line has flux blocking boundaries at each end and is embedded in a confining dielectric material, and if the line and confining material do not fail (i.e. the current density $\boldsymbol{j}$ is below some critical value), an equilibrium state of zero atomic flux ($\boldsymbol{J} = 0$) results along the line after sufficient time for the electromigration and stress driven diffusion terms to balance. Some studies proposed extensions to equation [3.1] including Park *et al.* (1999) who add the effect of alloying elements on the chemical potential driving force and Sarychev *et al.* (2000) who consider the effect of a non-equilibrium vacancy concentration field. In this chapter, we ignore these effects, which are typically second order, and only consider the basic equation [3.1].

As simple as equation [3.1] may appear, the effective use of this equation has been hampered by the fact that the average mass transport diffusion coefficient $D$ and the effective charge number $Z^*$ are difficult to accurately determine and because the relationship between the atomic flux $\boldsymbol{J}$ and the stress $\bar{\sigma}$ is not clear. The average mass diffusion coefficient $D$ is a difficult quantity to accurately determine as it depends on the diffusion paths, the activation energy associated with each active diffusion path, and, to a lesser degree, the stress state (Clement and Thompson 1995, Hu *et al.* 1999). The effective charge number $Z^*$ has proved to be difficult to determine both theoretically and experimentally. Researchers have made indirect measurements of $Z^*$ by either measuring the drift velocity associated with the atomic flux when there is no confinement and thus zero stress in equation [3.1] (Hu *et al.* 1999, Penney 1964) or by measuring the stress in conductor lines under steady-state conditions when the atomic flux is zero (Blech and Tai 1977, Wang *et al.* 1998). If there is no confinement, the drift velocity is:

$$\boldsymbol{v}_{\mathrm{d}} = -\frac{D}{kT} e\rho |Z^*| \boldsymbol{j} \qquad [3.2]$$

The difficulty with this approach is that the drift velocity is difficult to measure accurately and the diffusion coefficient $D$, as mentioned above, is not easily determined. If the conductor line is along the $y$ direction, then at steady state, equation [3.1] may be solved for $|Z^*|$ as:

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$$|Z^*| = \frac{\Omega}{e\rho j_y}\frac{\partial \bar{\sigma}}{\partial y} \qquad [3.3]$$

where $j_y$ is the $y$ component of the current density. All the terms in the right hand side of equation [3.3] are readily known or determined experimentally except the stress gradient. Measurement of the stress can only be done indirectly and is discussed in more detail in the next paragraph. The difficulty with relating the atomic flux $\boldsymbol{J}$ to the stress $\bar{\sigma}$ is based on the fact that although we can predict how much mass is accumulating or depleting at a point by taking the divergence of the atomic flux $\nabla \boldsymbol{J}$, how the diffusing mass arranges itself is not clear, but has an important effect on the stress state.

Furthermore, the stress is a tensor, and the scalar part of the stress that is the appropriate driving force in equation [3.1] is also not completely clear. In this chapter, we explore how modeling and simulation coupled with *in situ* X-ray microbeam experiments may be used to resolve or shed light on some of these difficulties.

The measurement of the stress state is critical to both the accurate determination of $Z^*$ and to shed light on the diffusion paths and how the diffusing mass arranges itself. In most cases, it is not possible to measure stress directly, but rather elastic deformation or strains are measured and, through knowledge of the elastic material behavior, the stress can be computed. One of the earliest attempts to measure the stress state during electromigration was by Blech and Tai (1977) who measured the deformation in a silicon substrate using X-ray topography to infer the stress distribution in an aluminum conductor line. Raman microscopy has been used to measure all six components of the strain distribution in the silicon substrate near the interconnect line, which together with a model of the interconnect line and surrounding substrate and passivation layer was used to infer the stress state in the line (Ma *et al.* 1995). In more recent years, convergent-beam electron diffraction (CBED) and Laue X-ray microdiffraction have made it possible to make direct measurements of strain within the interconnect line *in situ* during electromigration. CBED allows very high spatial resolution (20–100 nm), but requires samples to be thinned to electron transparency, thus altering the original stress state, and also only allows the measurement of two components of the strain (Nucci *et al.* 2005). X-ray microdiffraction has a lower spatial resolution (500–1000 nm) than CBED, but does not have the drawback of requiring thinned samples and has been applied directly to typical lines subjected to electromigration (Cargill III *et al.* 2006, Solak *et al.* 1999, Spolenak *et al.* 2001, Tamura *et al.* 2001, 2002, Valek *et al.* 2002, Wang *et al.* 1998, Zhang *et al.* 2008). With white-beam Laue X-ray microdiffraction, the five deviatoric, elastic strain components as well as the crystal orientation are measured, but the volumetric elastic strain, associated with the hydrostatic stress, cannot be determined. On the other

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hand, with a monochromatic beam and a conductor line with a <111> fiber texture, the elastic strain along the <111> direction may be determined by measuring the *d*-spacing using Bragg's law. With both a Laue white-beam and a Bragg monochromatic measurement, all components of the elastic strain as well as the orientation may be determined, which allows for direct calculation of all components of the stress tensor given the single crystal elastic parameters. Unfortunately, Bragg monochromatic microdiffraction measurements on polycrystalline thin films have been practical only for samples with strong crystallographic texture (Wang *et al.* 1989, Zhang *et al.* 2008). Therefore, in general, modeling and simulation must be used in conjunction with the measurements to determine the stress state and infer information about the physics that lead to the resulting stress and strain state.

## 3.2 Modeling and simulation approaches

### 3.2.1 Governing equations

In addition to equation [3.1] for the atomic flux, an equation relating the atomic flux to the resulting inelastic deformation resulting from the mass diffusion, governing equations for the material response that relate the inelastic deformation to the change in stress, and the stress equilibrium equation are needed. The divergence of the atomic flux is related to the rate of local, inelastic unit volume change (dilatation) as:

$$\frac{\partial \Delta^{\mathrm{em}}}{\partial t} = -\Omega \nabla \cdot \boldsymbol{J} \qquad [3.4]$$

where

$$\Delta^{\mathrm{em}} = tr(\boldsymbol{\varepsilon}^{\mathrm{em}}) \qquad [3.5]$$

and where *tr* is the trace operator and $\boldsymbol{\varepsilon}^{\mathrm{em}}$ is the electromigration induced inelastic strain tensor.

Assuming isothermal conditions and neglecting plasticity, the following equations of equilibrium and linear elasticity must be satisfied on the entire problem domain $V$ (including the conductor line and surrounding material):

$$\nabla \cdot \sigma = 0 \qquad [3.6]$$

$$\boldsymbol{\sigma} = \boldsymbol{\mathcal{L}} : \varepsilon^{\mathrm{e}} \qquad [3.7]$$

$$\boldsymbol{\varepsilon}^{\mathrm{e}} = \boldsymbol{\varepsilon} - \boldsymbol{\varepsilon}^{\mathrm{em}} \qquad [3.8]$$

$$\varepsilon = \frac{1}{2}\left(\nabla \boldsymbol{u} + \nabla \boldsymbol{u}^{\mathrm{T}}\right) \qquad [3.9]$$

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where $\boldsymbol{\sigma}$ is the stress tensor, $\boldsymbol{\mathcal{L}}$ is the fourth order elasticity tensor, $\boldsymbol{\varepsilon}^{e}$ and $\boldsymbol{\varepsilon}$ are the elastic and total strain tensors, and $\boldsymbol{u}$ is the displacement vector field. Note that $\boldsymbol{\varepsilon}^{em}$ is nonzero only in the conductor line. In addition, the following initial and boundary conditions are required for solution:

$$\Delta^{em} = \Delta_0^{em} \quad \text{at } t = 0 \quad \text{in } V^L \tag{3.10}$$

$$\boldsymbol{J} \cdot \boldsymbol{n}^L = 0 \quad \text{on } S^L \tag{3.11}$$

$$\boldsymbol{\sigma} \cdot \boldsymbol{n} = \hat{\boldsymbol{T}} \quad \text{on } S_1 \tag{3.12}$$

$$\boldsymbol{u} = \hat{\boldsymbol{u}} \quad \text{on } S_2 \tag{3.13}$$

where $t$ is time, $V^L \subset V$ is the part of the domain containing only the conductor line (where equation [3.1] is relevant) bounded by surface $S^L$ with outward unit normal $\boldsymbol{n}^L$, $\hat{\boldsymbol{T}}$ is a prescribed traction, and $S = S_1 \cup S_2$ is the boundary of $V$ with outward unit normal $\boldsymbol{n}$. Equation [3.10] indicates a prescribed initial value for the electromigration-induced volumetric strain, equation [3.11] indicates blocking boundaries on the conductor line surface, and equation [3.12] and [3.13] are the usual necessary traction and displacement boundary conditions for stress analysis.

Equations [3.1] and [3.4]–[3.9] and initial and boundary conditions [3.10]–[3.13] provide a framework for modeling stress evolution during electromigration, but require two additional equations. First, the scalar part of the stress tensor $\boldsymbol{\sigma}$, which acts as the driving stress $\bar{\sigma}$ in equation [3.1], needs to be defined. As mentioned earlier, the stress in this equation is sometimes taken as the hydrostatic stress, that is:

$$\bar{\sigma} = \frac{1}{3} tr(\boldsymbol{\sigma}) \tag{3.14}$$

or as the average normal stress on the grain boundaries, that is:

$$\bar{\sigma} = \langle \boldsymbol{n}^g \cdot \boldsymbol{\sigma} \cdot \boldsymbol{n}^g \rangle \tag{3.15}$$

where $\boldsymbol{n}^g$ is the normal to a grain boundary, and where < > indicates averaged over the grain boundaries in the neighborhood. If the grain structure is columnar and equi-axed in the plane, then $\bar{\sigma} = (\sigma_{xx} + \sigma_{yy})/2$, and if it is polycrystalline throughout, equation [3.14] is obtained. Second, from equation [3.4] we have an evolution equation for $\Delta^{em}$, which is related to the electromigration strain tensor in equation [3.5], but does not provide sufficient information to determine the entire electromigration strain tensor required for the stress analysis in equation [3.8]. Specifically, from equation [3.5], we know $\Delta^{em} = \varepsilon_{xx}^{em} + \varepsilon_{yy}^{em} + \varepsilon_{zz}^{em}$, but we do not have a relationship defining how to partition the electromigration-induced strain into components $\varepsilon_{xx}^{em}$, $\varepsilon_{yy}^{em}$, and $\varepsilon_{zz}^{em}$. The specific partition into components depends on how the diffusing atoms and vacancies arrange themselves, which, in turn,

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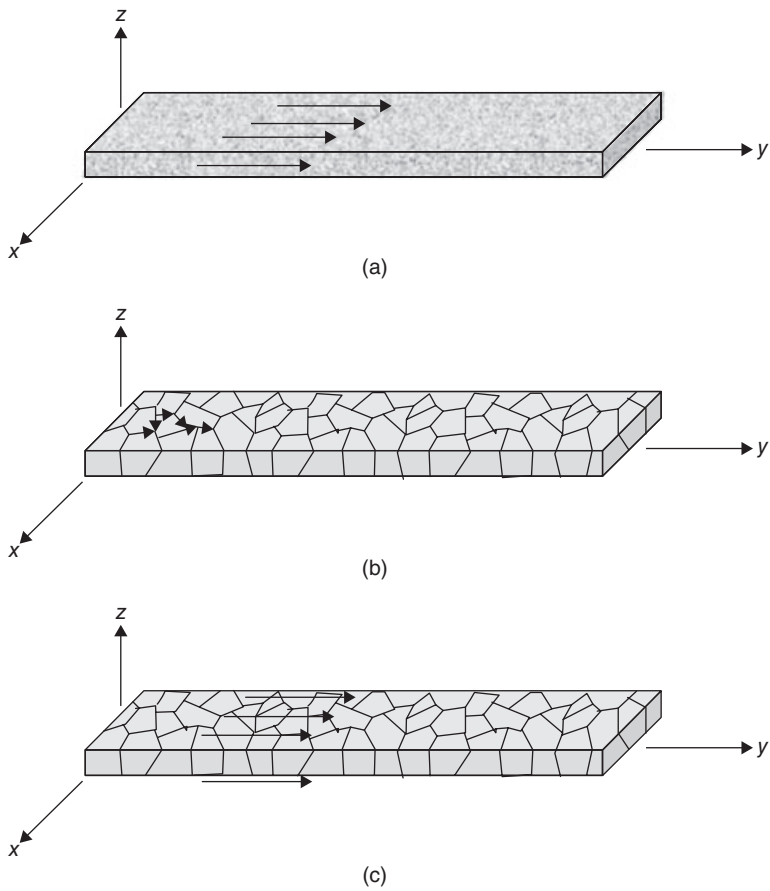
depends on the diffusion paths and the energy associated with the different possible configurations. Hau-Riege and Thompson (2000) investigated three different scenarios, which they associated with different dominant diffusion paths. Letting the interconnect line be along the $y$ direction with line width along $x$ and $z$ in the thickness direction or normal to the substrate (Fig. 3.1), these scenarios are:

$$(i) \quad \varepsilon_{xx}^{em} = \varepsilon_{yy}^{em} = \varepsilon_{zz}^{em} = \frac{\Delta^{em}}{3} \qquad [3.16]$$




*3.1* Illustration of three possible diffusion paths: (a) bulk diffusion through the volume or along the many grain boundaries in a polycrystalline line, (b) grain boundary diffusion through a columnar grain structure, and (c) surface diffusion along the top and bottom surfaces of a conductor line.

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where the material is assumed to be deposited or depleted equally in all three directions, which is associated with bulk diffusion or diffusion along grain boundaries in a polycrystalline line,

$$(ii) \quad \varepsilon_{xx}^{em} = \varepsilon_{yy}^{em} = \frac{\Delta^{em}}{2}, \quad \varepsilon_{zz}^{em} = 0 \qquad [3.17]$$

where material is deposited or depleted equally in the two in-plane directions, which is associated with diffusion along grain boundaries in a columnar grain structure, and

$$(iii) \quad \varepsilon_{zz}^{em} = \Delta^{em}, \varepsilon_{xx}^{em} = \varepsilon_{yy}^{em} = 0 \qquad [3.18]$$

where material is deposited or depleted in the thickness direction of the line, which is associated with diffusion along the top and bottom surfaces. It should also be noted that since the electromigration-induced mass flux leads to local changes in material volume, which is only associated with the diagonal elements of $\boldsymbol{\varepsilon}^{em}$, it is reasonable to assume that the off-diagonal elements remain zero. With the addition of either equation [3.14] or [3.15] and choosing one of equation [3.16]–[3.18] or some other relationship between the electromigration-induced strain components, together with the governing equations [3.1] and [3.4]–[3.9] and initial and boundary conditions in equations [3.10]–[3.13], it is possible to solve for the electromigration-induced strain $\boldsymbol{\varepsilon}^{em}$, the displacement field $\boldsymbol{u}$, the elastic strains $\boldsymbol{\varepsilon}^{e}$ and the stress $\boldsymbol{\sigma}$.

## 3.2.2 Analytical model

Korhonen *et al.* (1993) developed an analytic one-dimensional (1D) model that has been widely used. If we assume the interconnect line lies along the $y$ direction and that the current density $\boldsymbol{j}$ and atomic flux $\boldsymbol{J}$ are directed along $y$, then substituting equation [3.1] into equation [3.4] becomes:

$$\frac{\partial \Delta^{em}}{\partial t} = \frac{\partial}{\partial y}\left[\frac{D}{kT}\left(e\rho|Z^*|j_y - \Omega\frac{\partial \bar{\sigma}}{\partial y}\right)\right] \qquad [3.19]$$

Furthermore, if the conductor line is constrained and the material in both the conductor and the surrounding layers is assumed to be linear elastic as given in equation [3.7], then there is a linear relationship between the stress $\bar{\sigma}$ (regardless of how it is defined, equations [3.14] or [3.15]) and the electromigration-induced unit volume change $\Delta^{em}$, and thus,

$$\frac{\partial \bar{\sigma}}{\partial t} = -B\frac{\partial \Delta^{em}}{\partial t} \qquad [3.20]$$

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where $B$ is a constant and depends on the geometry and elastic properties of the conductor line and surrounding layers. Equations [3.19] and [3.20] then give the resulting 1D stress evolution equation

$$\frac{\partial \bar{\sigma}}{\partial t} = -B\frac{\partial}{\partial y}\left[\frac{D}{kT}\left(e\rho|Z^*|j_y - \Omega\frac{\partial \bar{\sigma}}{\partial y}\right)\right] \quad [3.21]$$

In order to use the above equation, an estimate of $B$ is required. Korhonen *et al.* (1993) approximated the cross-section of the line as an elliptical inclusion in a homogeneous medium and applied the Eshelby theory of inclusions (Eshelby 1957) to estimate $B$. From the Eshelby inclusion theory, the inelastic, electromigration-induced strain in the inclusion is related to the resulting stress in the inclusion by

$$\boldsymbol{\varepsilon}^{\mathrm{em}} = [(\mathcal{K} - \mathcal{I})^{-1}\mathcal{S}^{\mathrm{M}} + \mathcal{S}^{\mathrm{M}} - \mathcal{S}^{\mathrm{L}}]:\boldsymbol{\sigma} \quad [3.22]$$

where $\mathcal{K}$, $\mathcal{I}$, and $\mathcal{S} = \mathcal{L}^{-1}$ are the fourth order Eshelby identity, and compliance tensors, and superscripts $M$ and $L$ indicate the surrounding medium and the conductor line, respectively. If the surrounding matrix material (passivation layer) is assumed to be isotropic with elastic modulus $E_{\mathrm{M}}$ and Poisson's ratio $\nu_{\mathrm{M}}$ and the inclusion (conductor line) is treated as a face-centered-cubic material (e.g. aluminum or copper) with a strong <111> fiber texture and random in-plane texture (resulting in transversely isotropic symmetry about the $z$ axis), then the above relationship becomes

$$\begin{bmatrix}\varepsilon_{xx}^{\mathrm{em}}\\ \varepsilon_{yy}^{\mathrm{em}}\\ \varepsilon_{zz}^{\mathrm{em}}\end{bmatrix} = -\begin{bmatrix} \dfrac{2(1-\nu_{\mathrm{M}}^2)h}{E_{\mathrm{M}}w} + S_{11}^{\mathrm{L}} & S_{12}^{\mathrm{L}} & -\dfrac{(1-2\nu^{\mathrm{M}})(1+\nu^{\mathrm{M}})}{E_{\mathrm{M}}} + S_{13}^{\mathrm{L}} \\ S_{12}^{\mathrm{L}} & S_{11}^{\mathrm{L}} & S_{13}^{\mathrm{L}} \\ -\dfrac{(1-2\nu^{\mathrm{M}})(1+\nu^{\mathrm{M}})}{E_{\mathrm{M}}} + S_{13}^{\mathrm{L}} & S_{13}^{\mathrm{L}} & \dfrac{2(1-\nu_{\mathrm{M}}^2)w}{E_{\mathrm{M}}h} + S_{33}^{\mathrm{L}} \end{bmatrix}\begin{bmatrix}\sigma_{xx}\\ \sigma_{yy}\\ \sigma_{zz}\end{bmatrix} \quad [3.23]$$

where $w$ and $h$ are the width and thickness of the conductor line and $S_{ij}^{\mathrm{L}}$ are the components of the compliance matrix for the line. By substituting in equation [3.16], [3.17], or [3.18], on the left hand side of [3.23], the system may be solved for $\sigma_{xx}$, $\sigma_{yy}$, and $\sigma_{zz}$ in terms of $\Delta^{\mathrm{em}}$, and the parameter $B$, relating $\bar{\sigma}$ and $\Delta^{\mathrm{em}}$, may then be determined. Although the above approximate analytic model provides some valuable insight into the evolution of stress in the line and the effect of different potential diffusion paths, it is not able to quantitatively capture the effect of the real geometry with multiple material layers and lines with non-elliptic cross-sections.

### 3.2.3 Finite-element model

The finite-element method (FEM) allows for an accurate model of the geometry of the line and the consideration of multiple material layers. The

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Eshelby approximation of the cross-section derived above, for an elliptical inclusion in an infinite matrix, results in uniform stress and strain fields in the inclusion. However, if the inclusion is not elliptic, the stress and strain field in the inclusion is no longer uniform, and the finite element method is well-suited for determining these fields.

A finite-element formulation based on the governing equations presented in section 3.2.1 is as follows. Substituting equation [3.1] into equation [3.4] and taking the weak form yields:

$$\int_{V^{\mathrm{L}}} \frac{\partial \Delta^{\mathrm{em}}}{\partial t} \tilde{w} \mathrm{d}V = \int_{V^{\mathrm{L}}} \frac{D}{kT} (-e\rho |Z^*| \boldsymbol{j} + \Omega \nabla \bar{\sigma}) \cdot \nabla \tilde{w} \mathrm{d}V \qquad [3.24]$$

for the conductor line where $\tilde{w}$ is an arbitrary weighting function, and the blocking boundary condition equation [3.11] has been used. We can also write the usual weak form for the equilibrium and linear elastic equations [3.6]–[3.9] over the domain $V$:

$$\int_V (\boldsymbol{\mathcal{L}} : \nabla \boldsymbol{u}) : \nabla \boldsymbol{v} \, dV = \int_V (\boldsymbol{\mathcal{L}} : \boldsymbol{\varepsilon}^{\mathrm{em}}) : \nabla \boldsymbol{v} dV + \int_{S_1} \hat{\boldsymbol{T}} \cdot \boldsymbol{v} dS \qquad [3.25]$$

where $\boldsymbol{v}$ is an arbitrary vector valued weighting function that is zero on $S_2$. The above two equations, together with the initial condition equation [3.10] and boundary condition equation [3.13], can be discretized with the finite-element method in space and a central difference in time for equation [3.24] and solved for $\Delta^{\mathrm{em}}$ and $\boldsymbol{u}$ using a staggered approach. Specifically, letting $\Delta t$ be the time step and $n$ represent the current time increment, a discrete system of equations results of the form:

$$\frac{1}{2\Delta t} \mathbf{M} \left( \boldsymbol{\Delta}^{\mathrm{em}}_{\mathrm{n}+1} - \boldsymbol{\Delta}^{\mathrm{em}}_{\mathrm{n}-1} \right) = \mathbf{h}_{\mathrm{n}} \qquad [3.26]$$

$$\mathbf{K} \mathbf{u}_{\mathrm{n}+1} = \mathbf{f}_{\mathrm{n}+1} \qquad [3.27]$$

where equation [3.26] represents the discrete form of equation [3.24] with coefficient matrix $\boldsymbol{M}$, $\Delta^{\mathrm{em}}$ represents a vector of nodal values of the electromigration-induced dilatational strain, and right-hand-side vector $\boldsymbol{h}$ depends on the current density $\boldsymbol{j}$ and stress $\bar{\sigma}$ at time $t_{\mathrm{n}}$. Equation [3.27] is the discrete form of equation [3.25] with coefficient matrix $\boldsymbol{K}$, vector of nodal displacements $\boldsymbol{u}$, and right-hand-side vector $\boldsymbol{f}$ depending on the electromigration induced strain $\boldsymbol{\varepsilon}^{\mathrm{em}}$ and boundary traction $\hat{\boldsymbol{T}}$ at time $t_{\mathrm{n}+1}$. Thus, given information at the current time $t_{\mathrm{n}}$, equation [3.26] may be solved to update the electromigration-induced dilatational strain $\boldsymbol{\Delta}^{\mathrm{em}}$ at time $t_{\mathrm{n}+1} = t_{\mathrm{n}} + \Delta t$. Using this to define $\boldsymbol{\varepsilon}^{\mathrm{em}}_{n+1}$ and given prescribed boundary tractions $\hat{\boldsymbol{T}}_{\mathrm{n}+1}$, the displacement field can then be updated using equation [3.27] to time $t_{\mathrm{n}+1}$, which may, in turn, be used to solve for the updated stress using Equations [3.7]–[3.9], and thus, updating $\bar{\sigma}$ to be used in the next step

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in equation [3.26]. After sufficient time, a steady-state solution is reached where $\partial\Delta^{em}/\partial t = 0$ in equation [3.24] and

$$\nabla\bar{\sigma} = \frac{e\rho|Z^*|}{\Omega}\boldsymbol{j} \qquad [3.28]$$

## 3.3 Experimental, modeling and simulation findings

This section shows how X-ray microbeam experiments together with modeling and simulation, using the methods described in section 3.2, may be used to infer information about the diffusion paths and driving stresses active during electromigration. Here, we focus on two X-ray microbeam experimental studies on aluminum (Al) conductor lines with very different observations.

### 3.3.1 Experiments

The two experiments considered are documented by Wang *et al.* (1998) and Zhang *et al.* (2008). Cross-sectional diagrams for the lines in each experiment are shown in Fig. 3.2a and 3.2b, and a transmission electron microscopy (TEM) image of the cross-section from the Zhang *et al.* (2008) investigation is shown in Fig. 3.2(c). In the study by Wang *et al.* (1998), the elastic strain component $\varepsilon^e_{zz}$ was measured using energy-dispersive microbeam X-ray diffraction along the lengths of Al conductor lines that were 200 μm long, 10 μm wide, and 0.5 μm thick, with a 1.5 μm $SiO_2$ passivation layer and a Si (100) substrate. There was also a 10 nm Ti/60 nm TiN shunt layer under the line, which is not shown in Fig. 3.2. The grain structure in the Al lines was columnar with average grain size roughly the same as the film thickness and had a strong <111> fiber texture, with the <111> crystal direction preferentially oriented along the $z$ direction. The experimental temperature was 260 °C, and the current density was $1.4 \times 10^5$ A cm$^{-2}$. In that experiment, the strain $\varepsilon^e_{zz}$ was found to increase (become more tensile) linearly along the direction of electron flow. Zhang *et al.* (2008) measured both the elastic strain component $\varepsilon^e_{zz}$ (using Bragg monochromatic diffraction) and all the components of the elastic, deviatoric strain tensor $\boldsymbol{\varepsilon}^{e*} = \boldsymbol{\varepsilon}^e - \frac{1}{3}tr(\boldsymbol{\varepsilon}^e)(\boldsymbol{I})$ (using Laue white-beam diffraction) in separate experiments, throughout two Al conductor lines with nominally the same structure. The lines were approximately 30 μm long, 2.6 μm wide, and 0.75 μm thick, with a 0.7 μm $SiO_2$ passivation layer and a Si (100) substrate. The grain structure consisted of polycrystalline (<100 nm grain size), Ti-rich layers (probably mixture of Al and $TiAl_3$ resulting from reaction of originally thin Ti liner layers with the Al line) above and below the central part

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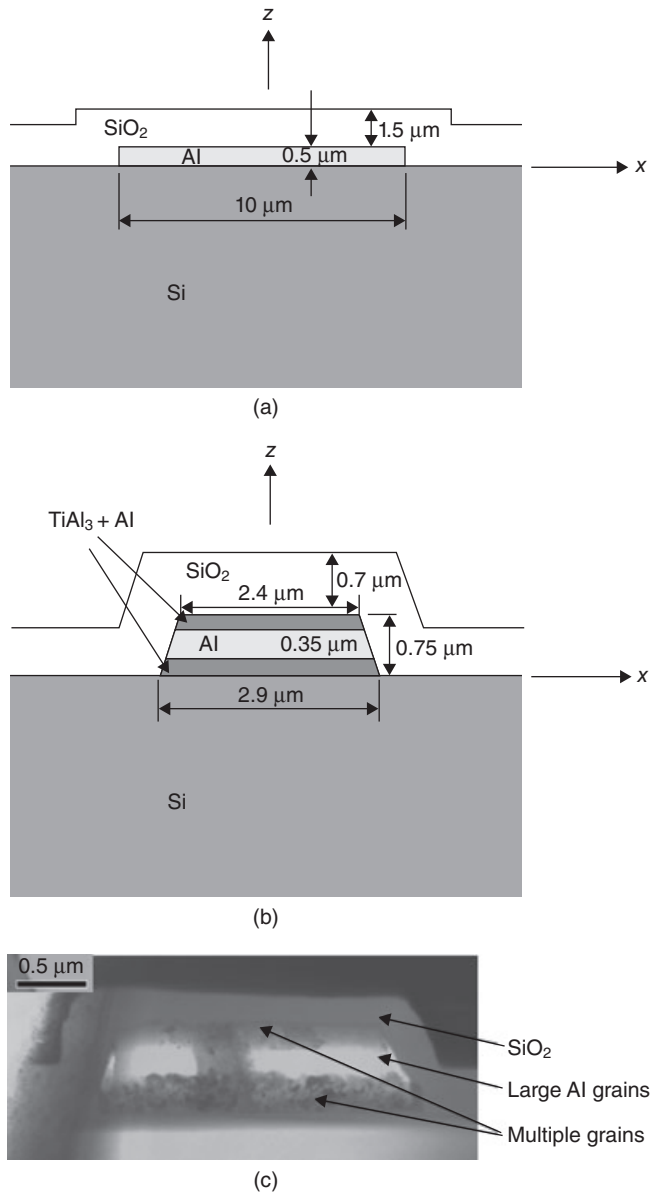


3.2 Schematic cross-sections for the two Al lines considered: (a) line investigated by Wang *et al.* (1998); (b) line by investigated Zhang *et al.* (2008); (c) TEM image of cross-section of line investigated by Zhang *et al.* (2008) showing small-grain polycrystalline layers on the top and bottom of the large grain Al line.

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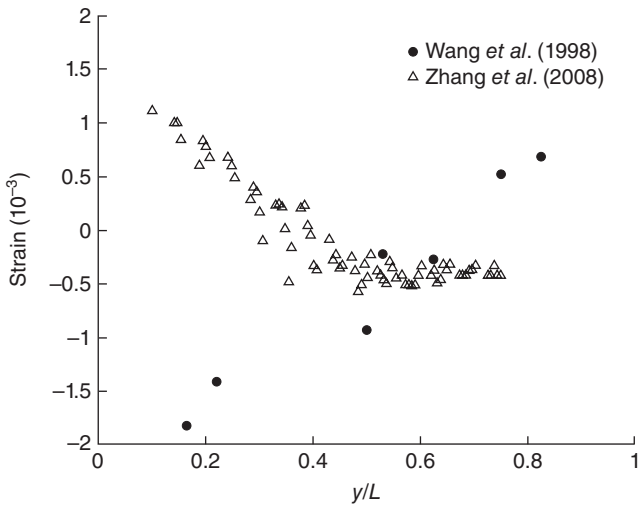
of the line, each about 0.2 μm thick, and micrometer-size columnar Al grains of about 0.35 μm thickness in the central part of the line, as can be seen in Fig. 3.2c. The experimental temperature was 190 °C and the applied current was 30 mA corresponding to a current density of $2.1 \times 10^6$ A cm$^{-2}$ if we assume the $TiAl_3$ takes up approximately 30% of the cross-sectional area and the current only travels through the Al part of the line as the resistivity of $TiAl_3$ is much higher than that of Al. In this experiment, the strain $\varepsilon^e_{zz}$ was found to decrease (become more compressive) linearly along the direction of electron flow to a point and then became constant. Fig. 3.3 shows a comparison of the measured elastic strains $\varepsilon^e_{zz}$ along the line lengths for the two experiments, showing the opposing trends.

For the line investigated by Zhang *et al.* (2008), the measured deviatoric strain components, $\varepsilon^{e*}_{yy}$ and $\varepsilon^{e*}_{zz}$, are shown in Fig. 3.4(a) and 3.4(b). Since $\varepsilon^{e*}_{xx} = -(\varepsilon^{e*}_{yy} + \varepsilon^{e*}_{zz})$, $\varepsilon^{e*}_{xx}$ is not shown here. The shear strains were also found to be relatively small and are also not shown. As observed for the full, elastic strain component $\varepsilon^e_{zz}$ in Fig. 3.3, a fairly linear trend is observed along the upstream end to about the middle of the line, but after this point, no clear trend is evident in the data, with a considerable amount of scatter appearing in the deviatoric data. In Zhang *et al.* (2008), the authors postulate that the passivation layer may have delaminated at the downstream end leading to




*3.3* A comparison of the measured elastic strain $\varepsilon^e_{zz}$ as a function of the normalized distance *y*/*L* along the line for the two Al lines considered here, where the electrons flow from left to right (current in –*y* direction).

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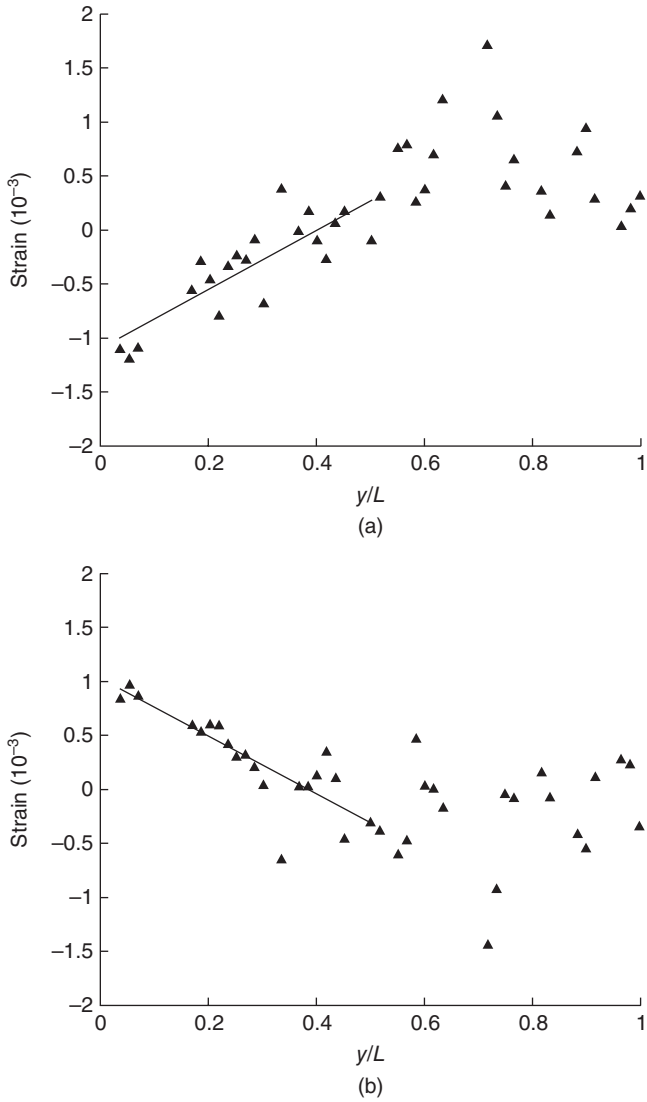
a drop in the stress. They also suggested that plastic deformation or recrystallization at the downstream end may have led to an increase in scatter. Therefore, the focus is on the upstream end here, where linear fits to the data are shown in Fig. 3.4(a) and 3.4(b).




*3.4* Measured elastic deviatoric strain components: (a) $\varepsilon^{e*}_{yy}$ and (b) $\varepsilon^{e*}_{zz}$ where $y/L$ is the normalized distance along the line (electrons flow left to right). Linear fits to the data are shown on the upstream end.

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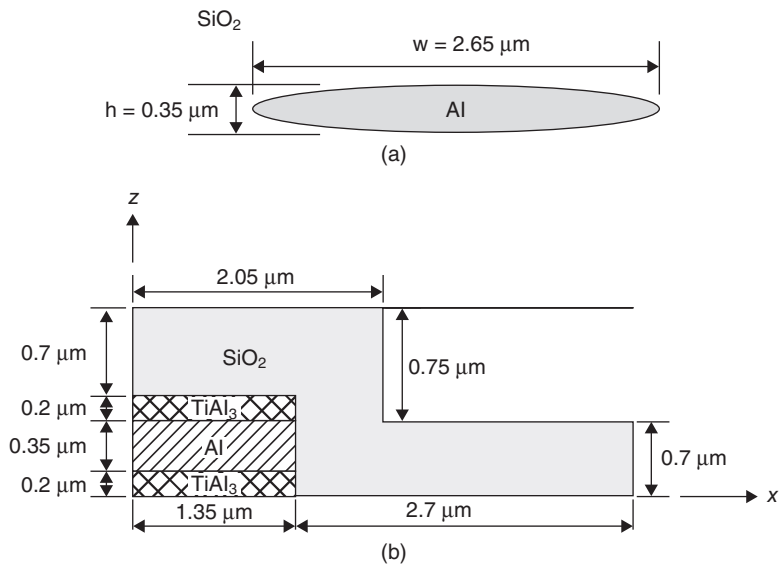
### 3.3.2 Eshelby and two-dimensional (2D) finite-element model findings

In order to start to understand the reason the two experiments described above exhibit opposite trends with regard to the elastic strain $\varepsilon^{e}_{zz}$, we compare the experimental results to results from two-dimensional (2D) cross-sectional models, where an inelastic, dilatational strain $\Delta^{em}$ prescribed in the line and each of the three scenarios for partitioning the strain given in equation [3.16]–[3.18] are considered.

*Findings for the Zhang* et al. *(2008) experiment*

Because we have measurements of all the components of the deviatoric, elastic strain as well as of the full, elastic strain component $\varepsilon^{e}_{zz}$ for the Zhang *et al.* (2008) experiment, we first focus on that case. The approximate models used are shown in Fig. 3.5(a) and 3.5(b), where symmetry about the $z$ axis is used in the finite-element model. Note that the Eshelby model approximates the line as an elliptic inclusion in an infinite matrix of the passivating material $SiO_2$ and, thus, does not accurately represent the geometry nor the




*3.5* 2D approximate models associated with the line cross-section in Fig. 3.2(b): (a) Eshelby model and (b) finite-element model geometry, where a symmetry boundary condition is taken about the $z$ axis and the Si substrate is treated as rigid.

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multiple layers of materials. The finite-element model here approximates the line geometry as rectangular rather than trapezoidal. The finite-element model also treats the Si substrate as effectively rigid, which from prior simulations has been found to be a reasonable approximation given the relatively large thickness of the substrate. Perfect bonding between the materials is also assumed (no relative sliding). The geometry shown in Fig. 3.5(b) is discretized into 1740 four-noded, bi-linear elements. The polycrystalline $SiO_2$ and the $TiAl_3$ are treated as isotropic with elastic moduli and Poisson's ratios of $E_s = 75$ GPa and $\nu_s = 0.17$ for the $SiO_2$ and $E_t = 170$ GPa and $\nu_t = 0.25$ for the $TiAl_3$. The Al is columnar and has a strong <111> texture, with the <111> direction preferentially oriented in the $z$ direction, and the in-plane texture is fairly random. Thus, the Al may be treated as transversely isotropic with the axis of symmetry aligned with the $z$ axis. The elastic stiffness parameters for the Al, computed from the single crystal properties at 190 °C, are $C_{11} = C_{22} = 107.1$ GPa, $C_{33} = 108.7$ GPa, $C_{12} = 59.2$ GPa, $C_{13} = C_{23} = 57.5$ GPa, $C_{44} = C_{55} = 22.3$ GPa, and $C_{66} = (C_{11} - C_{12})/2 = 23.9$ GPa.

Because the current direction is perpendicular to the cross-section, at steady state, from equation [3.28], the stress gradient in the cross-section should be zero ($\nabla\bar{\sigma} = 0$). For the Eshelby model, this is automatically satisfied since the Eshelby model predicts a uniform stress field in the inclusion (conductor line) for a uniform inelastic, electromigration-induced strain in the inclusion, which may be found using equation [3.23]. In the finite-element model, an initially uniform electromigration-induced dilatational strain $\Delta_0^{em}$ is prescribed in the Al line and then equations [3.26] and [3.27] are solved until the distribution of $\Delta^{em}$ in the cross-section is found such that $\nabla\bar{\sigma} = 0$. Each definition of $\bar{\sigma}$ given in equations [3.14] and [3.15] is considered as well as the three diffusion modes (*i*), (*ii*), and (*iii*) given in equation [3.16]–[3.18]. For the case where the stress $\bar{\sigma}$ is taken to be the normal stress to the grain boundaries, equation [3.15], the corresponding stress normal to the grain boundaries for each assumed diffusion mode is defined as:

$$(i) \quad \bar{\sigma} = \frac{1}{3} tr(\boldsymbol{\sigma}) \qquad [3.29]$$

where grain boundaries are assumed to be equally distributed in all directions (note, this is the same as the hydrostatic stress equation [3.14]),

$$(ii) \quad \bar{\sigma} = \frac{1}{2}(\sigma_{xx} + \sigma_{yy}) \qquad [3.30]$$

where the grains are assumed columnar and equi-axed, and

$$(iii) \quad \bar{\sigma} = \sigma_{zz} \qquad [3.31]$$

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where the diffusion is assumed to be primarily along the top and bottom faces.

First, the measured deviatoric, elastic strain components $\varepsilon_{xx}^{e*}$, $\varepsilon_{yy}^{e*}$, and $\varepsilon_{zz}^{e*}$ in the conductor line are compared with those predicted for each model. Because the elastic strain components are predicted to be proportional to $\Delta^{em}$, a direction associated with the normal strain components defined as:

$$d_x = \frac{\varepsilon_{xx}^{e*}}{\sqrt{\left(\varepsilon_{xx}^{e*}\right)^2 + \left(\varepsilon_{yy}^{e*}\right)^2 + \left(\varepsilon_{zz}^{e*}\right)^2}}$$
$$d_y = \frac{\varepsilon_{yy}^{e*}}{\sqrt{\left(\varepsilon_{xx}^{e*}\right)^2 + \left(\varepsilon_{yy}^{e*}\right)^2 + \left(\varepsilon_{zz}^{e*}\right)^2}} \tag{3.32}$$
$$d_z = \frac{\varepsilon_{zz}^{e*}}{\sqrt{\left(\varepsilon_{xx}^{e*}\right)^2 + \left(\varepsilon_{yy}^{e*}\right)^2 + \left(\varepsilon_{zz}^{e*}\right)^2}}$$

is used for comparison. Because the data is better for the upstream end, focus is on the upstream end where $\Delta^{em} < 0$. For the experiment, the direction components are computed at several locations along the upstream end, and an average value is used. For the finite-element cases, the average elastic strains in the line cross-section are used in computing $d_x$, $d_y$, and $d_z$. The experimental and simulation results for each case considered are given in Table 3.1. From Table 3.1, it can be seen that the mode (*i*) and mode (*ii*) models yield directions of the deviatoric, elastic strains that are nearly in the opposite direction from that observed in the experiment, whereas the mode (*iii*) simulations, which assume that material is depleted only in the thickness $z$ direction, give strains that are nearly in the same direction as

*Table 3.1* Comparison of the measured and predicted directions of the deviatoric, elastic strains. FEM (1) indicates finite-element model with gradient of the hydrostatic stress set to zero, and FEM (2) is when the gradient of the grain boundary stress is zero in the cross-section

| | $d_x$ | $d_y$ | $d_z$ |
|---|---|---|---|
| Experiment (Zhang *et al.* 2008) | 0.062 | –0.736 | 0.674 |
| Mode (*i*) Eshelby | 0.340 | 0.473 | –0.813 |
| Mode (*i*) FEM (1) and (2) | 0.342 | 0.472 | –0.812 |
| Mode (*ii*) Eshelby | 0.328 | 0.484 | –0.812 |
| Mode (*ii*) FEM (1) | 0.337 | 0.475 | –0.813 |
| Mode (*ii*) FEM (2) | 0.333 | 0.479 | –0.812 |
| Mode (*iii*) Eshelby | 0.509 | –0.807 | 0.289 |
| Mode (*iii*) FEM (1) | –0.143 | –0.625 | 0.767 |
| Mode (*iii*) FEM (2) | –0.094 | –0.656 | 0.749 |

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the experiment. From this we may conclude that the primary diffusion path for this experiment is probably through the interfaces between the columnar Al grains and the small $TiAl_3$ grains. Of the mode (*iii*) simulations, the FEM (2) simulation gives the best result, which corresponds to the case where $\bar{\sigma}$ is defined according to equation [3.31], i.e. the case where the driving stress is assumed to be the normal stress relative to the top and bottom surfaces which are considered the primary diffusion paths. The angle between the experimental direction and the mode (*iii*) FEM (2) direction is 10.9°. The mode (*iii*) FEM (1) case gives a result that is nearly as good with an angle between the experiment and simulation of 14.5°. For the mode (*iii*) Eshelby case, the angle between the experiment and simulation is 34.3°, which is not as good quantitatively as the FEM simulations, but is still considerably closer than any of the mode (*i*) or mode (*ii*) simulations. Thus, the Eshelby approximation may be a good way to determine which is the dominant diffusion path, but a finite-element simulation is necessary for good quantitative agreement.

The finite-element simulation also allows for the computation of the non-uniform distribution through the cross-section of the electromigration-induced volumetric strain $\Delta^{em}$, which is required to give a uniform $\bar{\sigma}$ in the cross-section. For the mode (*iii*) FEM (2) case, the normalized distribution of $\Delta^{em}$ is shown in Fig. 3.6(a) and 3.6(b). From these figures, we can see that more of the depleted (upstream, $\Delta^{em} < 0$) or deposited (downstream, $\Delta^{em} > 0$) material occurs towards the central part of the line (near $x = 0$), with much less material flowing to or from the edges (near $x = \pm 1.35$ μm).

From the curve fits to the experimental data on the upstream end, shown in Fig. 3.4(a) and 3.4(b), the magnitude of the deviatoric, elastic strain, which was used to normalize the deviatoric elastic strain components in equation [3.32], may be computed along the line length on the upstream end. By multiplying the magnitude of the deviatoric strain by the direction predicted in the mode (*iii*) FEM (2) simulation (Table 3.1), the deviatoric, elastic strain components along the upstream end of the line may be computed, and these are shown in Fig. 3.7(a) and 3.7(b) with the experimental data. Furthermore, because the model predicts the elastic strains to be proportional to the electromigration-induced dilatational strain $\Delta^{em}$, the average $\Delta^{em}$ may be determined along the length of the line for the upstream end, and from this, the full elastic strain $\varepsilon^{e}_{zz}$ may be computed along the length for the upstream end from the simulation, which is shown compared with the experimental data in Fig. 3.8. The simulation prediction is slightly higher on average than the experimental trend, but in reasonable agreement.

Lastly, we can use the simulation results to estimate $|Z^*|$. From the finite element simulation result, we can determine the ratios $\langle \varepsilon^{e}_{zz} \rangle / \langle \Delta^{em} \rangle$ and $B = -\bar{\sigma} / \langle \Delta^{em} \rangle$, where $B$ is the parameter appearing in equation [3.21] and where

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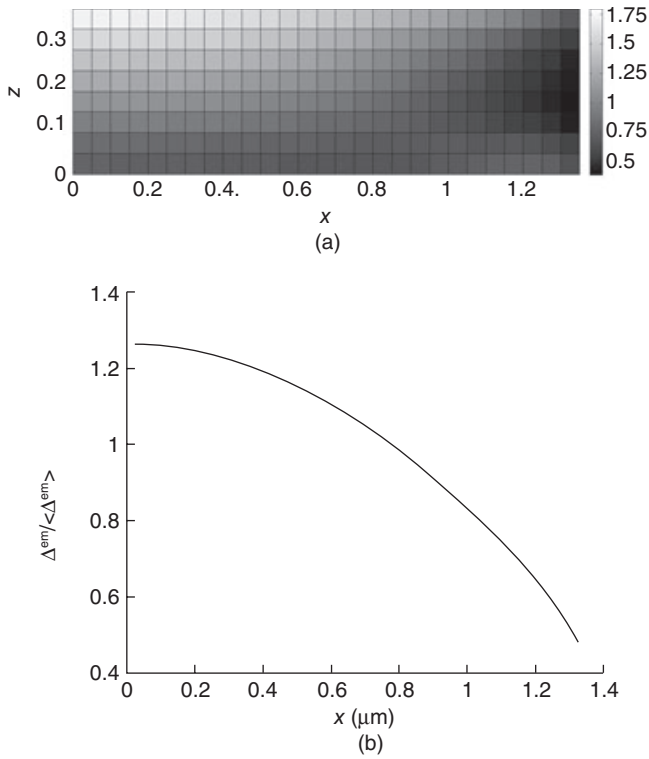


*3.6* Distribution of the electromigration-induced volumetric strain $\Delta^{em}$ normalized by the average of this strain $\langle\Delta^{em}\rangle$: (a) throughout the cross-section of the Al line ($x$ and $z$ in μm), and (b) from the middle to the edge of the line in the width direction averaged through the thickness.

the angle brackets indicated averaged over the cross-section. Fitting the measured strain component $\varepsilon^{e}_{zz}$, shown in Fig. 3.3, to a straight line, the slope $\partial\langle\varepsilon^{e}_{zz}\rangle/\partial y$ can be determined. Then the stress gradient may be determined from:

$$\frac{\partial\bar{\sigma}}{\partial y}=\frac{\bar{\sigma}}{\langle\Delta^{em}\rangle}\frac{\langle\Delta^{em}\rangle}{\langle\varepsilon^{e}_{zz}\rangle}\frac{\partial\langle\varepsilon^{e}_{zz}\rangle}{\partial y}=-B\frac{\langle\Delta^{em}\rangle}{\langle\varepsilon^{e}_{zz}\rangle}\frac{\partial\langle\varepsilon^{e}_{zz}\rangle}{\partial y} \qquad [3.33]$$

and used in equation [3.3] to find $|Z^*|$. The predicted stress gradient along the line length is $\partial\bar{\sigma}/\partial y = -17.9$ MPa μm$^{-1}$ when the driving stress is taken as the interface stress given in equation [3.31] and $\partial\bar{\sigma}/\partial y = -13.6$ MPa μm$^{-1}$ when the driving stress is taken as the hydrostatic stress given in equation [3.14]. Using equation [3.3] and $e = 1.602 \times 10^{-19}$ C, $\rho = 4.54 \times 10^{-6}$ ohm cm for Al at 190 °C, $\Omega = 1.66 \times 10^{-23}$ cm$^3$, and the current density estimated in

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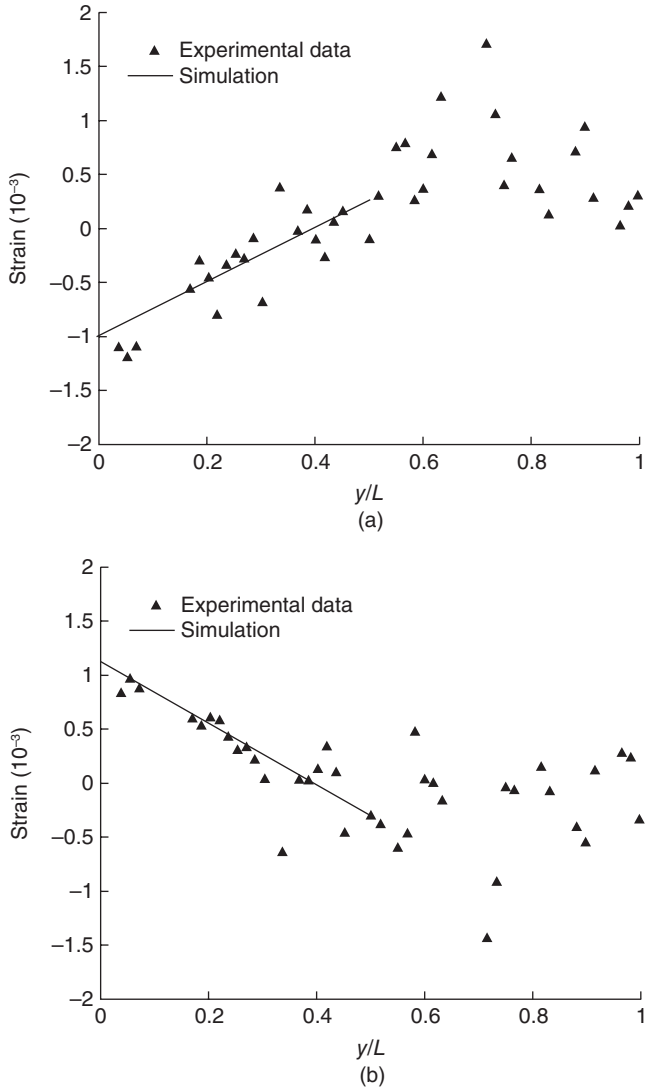


*3.7* Comparison of the measured deviatoric, elastic strains along the line with that computed using the simulation direction for the components (a) $\varepsilon^{e*}_{yy}$ and (b) $\varepsilon^{e*}_{zz}$.

section 3.3.1 of $j_y = -2.1 \times 10^6$ A cm$^{-2}$ (current flows in $-y$ direction), $|Z^*| = 1.94$ is obtained if the driving stress is the interface stress and $|Z^*| = 1.45$ if it is the hydrostatic stress. The latter number is similar to other reported findings for $|Z^*|$ in Al conductor lines, which typically fall in the range of 1.2–1.6 (Blech and Tai 1977, Wang *et al.* 1998, Chiras and Clarke 2000).

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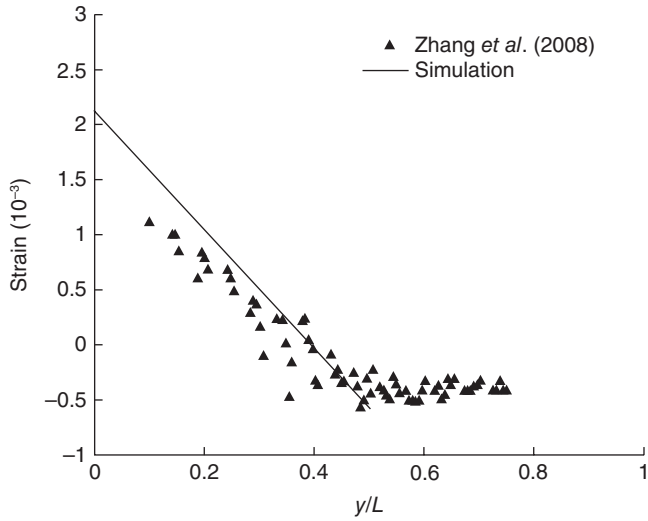


*3.8* A comparison of the measured elastic, out-of-plane strain $\varepsilon_{zz}^{e*}$ along the line with that computed from the simulation. The simulation predictions are based on the same linearly varying average $\Delta^{em}$ along the Al line length associated with the simulated strains in Figs. 3.7(a) and 3.7(b).

*Findings for the Wang* et al. *(1998) experiment*

For the experimental results given in Wang *et al.* (1998), we only have one measured elastic strain component, $\varepsilon_{zz}^{e}$, as shown in Fig. 3.3. As in the previous case, 2D Eshelby and finite-element models were created for this experimental geometry, shown in Fig. 3.2(a), where now the Eshelby model is the same as shown in Fig. 3.5(a), but with $w = 10$ μm and $h = 0.5$ μm. The finite element model geometry is the same as the geometry in the schematic, Fig. 3.2(a), but, as in the previous analysis, without the Si substrate, which is treated as a rigid foundation, and modeling only half the geometry taking advantage of the symmetry about the $z$ axis. The finite-element model was discretized with 3650 four-noded, bi-linear elements. The same properties for the Al and $SiO_2$ as in the previous example are used.

From the 2D Eshelby and finite-element simulations, we can determine, for the different diffusion modes and assumed driving stress definitions, the stress and elastic strain fields in the line cross-section that result from a unit of electromigration-induced dilatational strain in the cross-section. Thus, as in the previous example, we can determine the ratios $\langle\varepsilon_{zz}^{e}\rangle/\langle\Delta^{em}\rangle$ and $B = -\bar{\sigma}/\langle\Delta^{em}\rangle$, and use this information together with the slope $\partial\langle\varepsilon_{zz}^{e}\rangle/\partial y$, determined from fitting the data in Fig. 3.3, to compute the stress gradient. Then, $\langle Z^{*}\rangle$ is found using equation [3.3], where $e$ and $\Omega$ are the same as used in the

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*Table 3.2* Results associated with the Wang *et al.* (1998) data

| | $\frac{\langle \varepsilon_{zz}^{e} \rangle}{\langle \Delta^{em} \rangle}$ | $B$ (GPa) | $\frac{\partial \bar{\sigma}}{\partial y}$ | $\lvert Z^* \rvert$ |
|---|---|---|---|---|
| Mode (*i*) Eshelby (1) and (2) | 0.322 | 23.9 | −1.37 | 1.8 |
| Mode (*i*) FEM (1) and (2) | 0.329 | 23.5 | −1.32 | 1.8 |
| Mode (*ii*) Eshelby (1) | 0.487 | 31.9 | −1.32 | 1.8 |
| Mode (*ii*) Eshelby (2) | 0.487 | 51.4 | −1.94 | 2.6 |
| Mode (*ii*) FEM (1) | 0.503 | 34.5 | −1.26 | 1.7 |
| Mode (*ii*) FEM (2) | 0.501 | 51.1 | −1.88 | 2.5 |
| Mode (*iii*) Eshelby (1) | −0.00897 | 1.95 | 4.00 | |
| Mode (*iii*) Eshelby (2) | −0.00897 | 1.96 | 4.03 | |
| Mode (*iii*) FEM (1) | −0.00658 | 0.48 | 1.34 | |
| Mode (*iii*) FEM (2) | −0.00621 | 0.67 | 1.99 | |

previous case, the current density is $j_y = -1.4 \times 10^5$ A cm$^{-2}$, and $\rho = 5.5 \times 10^{-6}$ ohm-cm for Al at 260 °C. The model results are given in Table 3.2, where modes (*i*), (*ii*), and (*iii*), as before, refer to the considered diffusion modes described in equations [3.16]–[3.18], and (1) refers to considering the hydrostatic stress as the driving stress and (2) the grain boundary stress. From the results, we can first observe that mode (*iii*), where material is assumed to be deposited only in the $z$ direction, is not a viable mode because it predicts a positive slope in the stress and thus, a negative $|Z^*|$, which is not possible. Therefore, mode (*iii*) is ruled out as a possible diffusion mode. The remaining cases all predict values of $|Z^*|$ between 1.7 and 2.6. In Wang *et al.* (1998), the likely primary diffusion path was identified as being along the columnar grain boundaries with material deposited equally in $x$ and $y$, the mode (*ii*) assumption. Assuming an equi-biaxial stress in the film, and assuming the hydrostatic stress as the driving stress, they found $|Z^*| = 1.6$, which is close to values of 1.8 and 1.7 found here with the mode (*ii*) Eshelby and finite-element simulations, respectively. It is interesting to note that the Eshelby and the finite element simulations give very similar results for this particular cross-section geometry, where the line is relatively wide and only the Al line and the $SiO_2$ passivation layer are considered in the models.

## 3.4 Conclusions

Modeling and simulation coupled with X-ray microbeam measurement of elastic strains in conductor lines can be used to resolve some of the challenging questions regarding the physics of electromigration. Three key questions discussed here are:

1. How does the diffusing mass arrange itself and what does this imply about the dominant diffusion paths?

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2. What is the appropriate driving stress for electromigration, hydrostatic or grain boundary/interface stress?
3. What is the effective charge number $|Z^*|$?

For the two Al conductor line geometries considered here, the diffusing mass was determined to arrange itself very differently, with the material deposition/depletion in the line thickness ($z$) for the Zhang *et al.* (2008) case and in the width and length ($x$ and $y$) for the Wang *et al.* (1998) case. From these results, it may be concluded that for the Zhang *et al.* (2008) case, the primary diffusion path is probably along the top and bottom interfaces between the large columnar Al grains and the small polycrystalline $TiAl_3$ layers, whereas for the Wang *et al.* (1998) case, where the line is much wider with more Al columnar grain boundaries and much thinner $TiAl_3$ layers, it is probable that the columnar grain boundaries were the primary diffusion path. As far as the appropriate driving stress, the results are not as clear. The Laue white-beam microdiffraction measurements, where all the components of the deviatoric, elastic strain are measured, provides sufficient data to investigate the driving stress by comparing the measured and computed directions of the deviatoric, elastic strains. From the Zhang *et al.* (2008) data, when the driving stress was assumed to be the stress normal to the primary diffusion interfaces, the computed direction of the deviatoric, elastic strain was slightly closer to the measured direction than that found when using the hydrostatic stress as the driving stress. More studies would be needed to make a conclusive statement. When the driving stress was assumed to be the grain boundary or interface stress normal to the primary diffusing paths, $|Z^*|$ was found to be 1.94 from the Zhang *et al.* (2008) data and 2.5 from the Wang *et al.* (1998) data, and when the hydrostatic stress was used as the driving stress in the analysis, $|Z^*|$ was found to be 1.45 from the Zhang *et al.* (2008) data and 1.7 from the Wang *et al.* (1998) data. Because the primary diffusion paths were different types of material interfaces for the two cases considered, the value of $|Z^*|$ may not be the same. Additional studies are needed to clarify the question of the driving stress and to pin down $|Z^*|$. The approach described here can be used to answer these questions, not only in aluminum interconnects, but also in copper. Three-dimensional finite element analyses could also provide additional insight, in particular about the validity of the plane strain assumption assumed here and time dependent behavior along the line direction.

## 3.5 Acknowledgments

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# 4

# X-ray microbeam analysis of electromigration in copper interconnects

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**Abstract**: Electromigration in Cu interconnect materials raises reliability issues and attention from microelectronics industries. Electromigration causes the formation of defects such as voids and hillocks, which can cause reliability problems such as opens or shorts. The formation of defects is associated with the evolution of strain/stress within the Cu interconnect materials. Measurements of strain/stress in Cu interconnects during electromigration advances the understanding of electromigration failure modes and helps in modeling electromigration mechanisms. In this chapter, we describe the background of X-ray microbeam analysis and discuss results from measurements made at the Advanced Photon Source, where a white beam X-ray of 0.5 μm size was used to study strain evolution during electromigration in Cu conductor lines.

**Key words**: electromigration, Cu interconnects, X-ray microbeam analysis, strain evolution.

## 4.1 Introduction

Because of its excellent mechanical, electrical and thermal properties, Cu has been extensively used as an interconnect material in the microelectronics industry. Better electromigration (EM) resistance is expected in Cu than in Al as interconnect materials, because Cu has higher thermal conductivity, higher melting temperature, and lower electrical resistivity than Al. However, EM in Cu interconnects remains a major cause of failure in microelectronic devices. With the scaling down of the dimensions of electronic devices, current densities are increased, heat dissipation become less efficient, and EM becomes more important as a failure mechanism.[1,2] EM causes depletion of atoms in the upstream area of electron flow and accumulation of atoms at the downstream area of electron flow along the conductor lines. A consequence of EM is that voids form in the upstream area and extrusions form in the downstream area. Figure 4.1 shows the microstructure of a Cu conductor line after an EM test with a current density of $1.6 \times 10^6$ A cm$^{-2}$ at 300 °C for 70 h. A void forms at the upstream, cathode end, and a hillock or extrusion forms at the downstream, anode end. EM can result in changes in resistance and can lead to open or short



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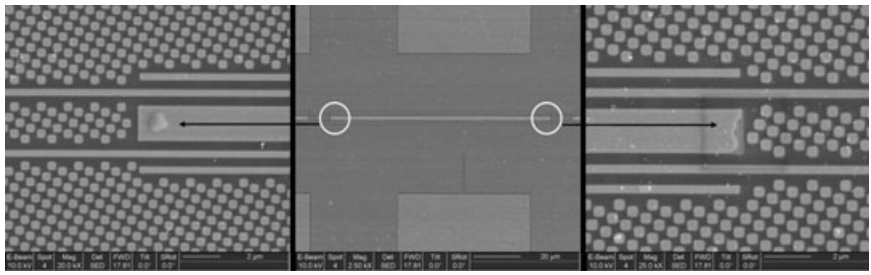

*4.1* SEM images of a Cu conductor line after EM test with electrons flowing from right to left. A void forms at the cathode end, and a hillock forms at the anode end.

circuit failures.[3] Studying the EM-induced strains in Cu conductor lines helps advance understanding of the EM mechanisms and can provide valuable information for semiconductor industries in developing better EM resistance components and, thus, more reliable products.

Traditional large beam X-ray strain measurements in thin film materials use a monochromatic X-ray source, with a specific wavelength (Cu or Co $K_\alpha$ X-ray, etc.), and use Bragg's law to determine the lattice spacing in the crystalline thin-film materials. The elastic strains are calculated from changes in lattice spacings. Uncertainties in the strain-free lattice spacings, which depend on temperature and impurity content, are a source of uncertainties in the measured strains. Wafer curvature measurement is another way to determine strains of thin-film materials on substrates. Both traditional large beam X-ray diffraction and wafer curvature measurements provide average strain values, for the area of the film covered by the X-ray beam for X-ray diffraction measurements, or for the entire thin film for wafer curvature measurements. Covergent-beam electron diffraction (CBED) and electron backscattering diffraction (EBSD) can provide high spatial resolution measurements of strains in conductor lines with line widths in the range of micrometers or sub-micrometers. Nucci *et al.*[4] have successfully used CBED for in situ measurement of strain evolution in an Al conductor line with line width below 1 μm. However, owing to the limited penetration depth of electrons, strain measurement using CBED or EBSD techniques is practical only in conductor lines without passivation layers, which is very different from current interconnect technology.

Third-generation synchrotron X-ray sources provide enough brightness for microdiffraction strain measurements with spatial resolution below 1 μm. Strain measurements for individual grains, or even within a single grain, are possible. Strain evolution measurements on Cu conductor lines during EM can be made for Cu lines with micrometer or submicrometer line widths. White beam X-ray Laue diffraction provides a method for

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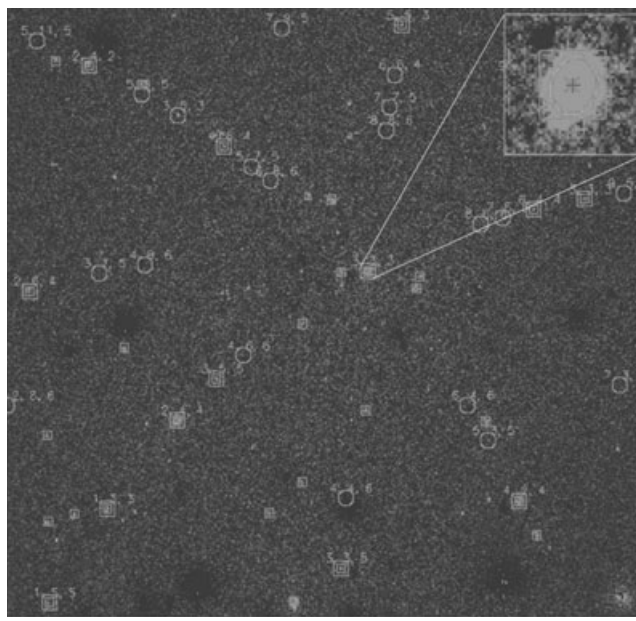
measuring local deviatoric strain tensors $\varepsilon_{ij}^{*}$, which are related to the usual full strain tensors $\varepsilon_{ij}$

$$\varepsilon_{ij}^{*} = \begin{bmatrix} \varepsilon_{xx}^{*} & \varepsilon_{xy}^{*} & \varepsilon_{xz}^{*} \\ \varepsilon_{yx}^{*} & \varepsilon_{yy}^{*} & \varepsilon_{yz}^{*} \\ \varepsilon_{zx}^{*} & \varepsilon_{zy}^{*} & \varepsilon_{zz}^{*} \end{bmatrix} = \begin{bmatrix} \varepsilon_{xx} - \dfrac{\Delta}{3} & \varepsilon_{xy} & \varepsilon_{xz} \\ \varepsilon_{yx} & \varepsilon_{yy} - \dfrac{\Delta}{3} & \varepsilon_{yz} \\ \varepsilon_{zx} & \varepsilon_{zy} & \varepsilon_{zz} - \dfrac{\Delta}{3} \end{bmatrix} \quad [4.1]$$

where $\Delta = \varepsilon_{xx} + \varepsilon_{yy} + \varepsilon_{zz}$ is the hydrostatic strain. For the usual choice of co-ordinate axes for thin film samples, $\varepsilon_{xx}^{*}$ and $\varepsilon_{yy}^{*}$ are the in-plane deviatoric strains and $\varepsilon_{zz}^{*}$ is the perpendicular deviatoric strain. The sum of the diagonal terms of the deviatoric strain tensor is zero,

$$\varepsilon_{xx}^{*} + \varepsilon_{yy}^{*} + \varepsilon_{zz}^{*} = 0 \quad [4.2]$$

In Laue microbeam X-ray diffraction, a CCD area detector is used to collect the Laue diffraction patterns. Figure 4.2 shows a Laue diffraction pattern from a single grain in a Cu thin-film sample. By analyzing the Laue patterns, the orientation and deviatoric strain tensor of each individual



*4.2* A Laue white beam X-ray diffraction pattern from a Cu grain, with an enlargement of the (333) Laue diffraction spot.[5]

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grain irradiated by X-rays, but not the hydrostatic strain, can be obtained. Detailed descriptions of analysis methods are available.[6,7]

## 4.2 Samples and X-ray microdiffraction methods

### 4.2.1 Copper conductor line samples

The Cu conductor lines used for microbeam X-ray strain measurements during EM described in this chapter were made by electrodeposition and patterned by the dual damascene process using chemical mechanical polishing (CMP).[8] An optical image of a Cu line sample is shown in Fig. 4.3(a). On the same Si substrate, there are four identical sections of Cu lines, and each section contains three Cu lines in series. The Cu lines are 0.45 μm thick, 2 μm wide and 100 μm long, with dielectric and passivation layers. There are vias between each pair of Cu lines. The $SiO_2$ passivation layer is 0.4 μm thick. A SEM image and schematic cross-section drawing of the Cu line are shown in Fig. 4.3(b) and 4.3(c). The grain size of the Cu line is similar to its thickness, ~0.5 μm.

### 4.2.2 X-ray microdiffraction experiments

Figure 4.4 shows a schematic of the experimental setup used at the Advanced Photon Source (APS) on beamline 34-ID. A photograph of the setup is shown in Fig. 4.5. Polychromatic X-rays from the synchrotron are focused by a set of K-B mirrors to form a microbeam of 0.5 μm diameter, which is diffracted from grains in the Cu line. The Cu line sample surface is oriented about 45 ° with respect to the incident X-ray beam. The CCD detector that collects the Laue diffraction patterns is above the Cu line sample, as shown in Fig. 4.4 and 4.5. The CCD and incident X-ray beam are fixed, and the sample stage is translated in directions along and across the Cu line, so that strain mapping of the entire Cu line is obtained. Cu fluorescence produced by the incident beam is used for sample alignment, as shown in Fig. 4.6.

### 4.2.3 X-ray microdiffraction strain measurement uncertainties

X-ray microdiffraction has been successfully applied to measure the strains for thin-film materials since 1998.[11–15] However, few studies were focused on the measurement uncertainty. To estimate the measurement uncertainty using microbeam diffraction and Laue pattern indexing as described in 4.1, repeated strain mappings on the same Al conductor line, without EM, were carried out. Each strain mapping contains 1573 measurements along and

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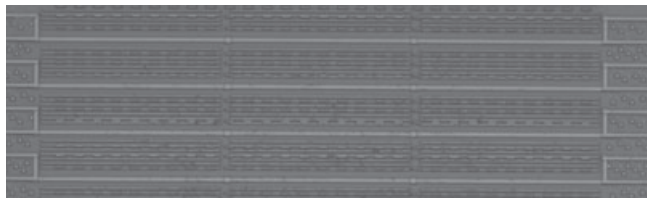
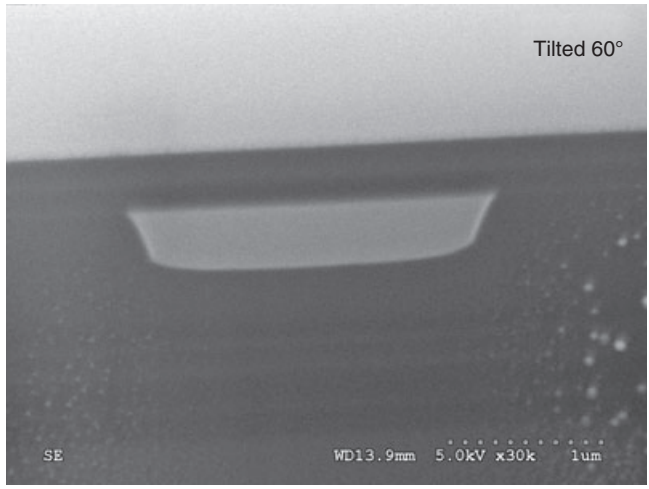
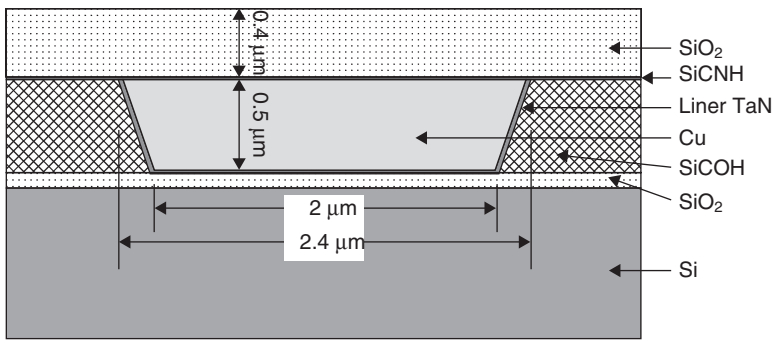


(a)




(b)




(c)

*4.3* (a) Optical image of the Cu line sample.[5] (b) SEM image of the cross-section of the Cu line after focused ion beam (FIB) milling.[9] (c) Schematic sketch of the cross-section of the Cu line.[10] (For (b) and (c): copyright © 2010 Materials Research Society. Reprinted with the permission of Cambridge University Press.)

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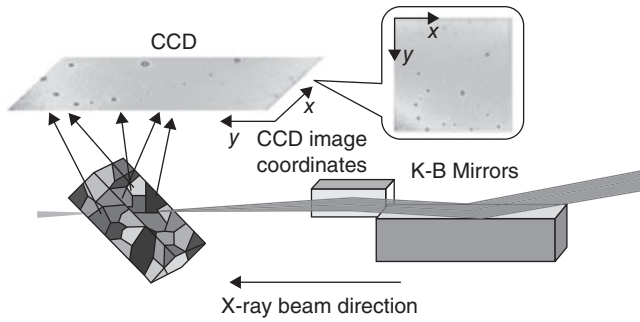
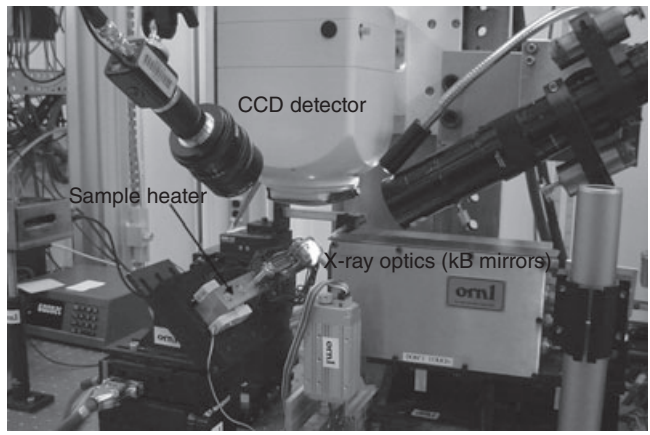
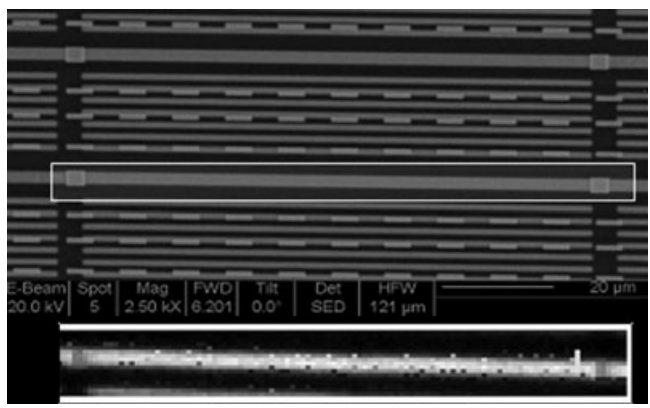



*4.4* Schematic setup for X-ray microdiffraction experiments using a polychromatic X-ray beam.[5]




*4.5* Setup of X-ray microbeam diffraction and heating stage.[5]




*4.6* Top: SEM image of the Cu line; the white rectangle shows the area scanned by X-rays. Bottom: Cu fluorescence map showing where the X-rays are incident on the Cu line.[5]

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*Table 4.1* Estimated uncertainties of white beam deviatoric strain measurement

| | $\varepsilon^*_{xx}$ | $\varepsilon^*_{yy}$ | $\varepsilon^*_{yy}$ |
|---|---|---|---|
| $\lambda_{11}(10^{-6})$ | 0.07 | 0.15 | 0.09 |
| $\lambda_{22}(10^{-6})$ | 0.07 | 0.10 | 0.06 |
| $\lambda_{12}(10^{-6})$ | 0.05 | 0.06 | 0.04 |
| Uncertainty $\Delta\varepsilon(10^{-3})$ | 0.14 | 0.25 | 0.19 |

across the line. The measurement uncertainty can be estimated as equation [4.3]

$$\Delta\varepsilon = \sqrt{\frac{1}{2}(\lambda_{11} + \lambda_{22}) - \lambda_{12}} \qquad [4.3]$$

where $\Delta\varepsilon$ is the strain measurement uncertainty, $\lambda_{11}$ is the self-correlation coefficient in the first strain mapping, $\lambda_{22}$ is the self-correlation coefficient in the second strain mapping and $\lambda_{12}$ is the correlation coefficient between the first and the second strain mappings. Detailed calculations for determination of the measurement uncertainty are shown in 4.6 Appendix. The calculated uncertainties are summarized in Table 4.1, with the uncertainties level ~$2 \times 10^{-4}$ for these strain measurements.

## 4.3 Electromigration (EM)-induced strains in conductor lines

### 4.3.1 Electron wind force and back flow strain gradient

Electromigration (EM) is the movement of atoms caused by current flowing in conductor lines. Atom movements are usually in the same direction as the electron flow. The driving force for the atomic diffusion is the electron flow, or electron wind force, in which the electrons transfer momentum to atoms.[16] EM normally occurs at elevated temperature and high current density. Study of EM-induced strain is normally carried out at higher temperature and higher current density than the usual service conditions of integrated circuit devices, to allow the failure or significant strain evolution to develop and be measured in a reasonably short period of time. An expression for the atom flux $J$ during EM, based on the initial proposal by Blech,[17] is shown in equation [4.4]:

$$J = n\frac{D_{\text{eff}}}{kT}\left[Z^* ej\rho - b\frac{\partial\sigma_{\text{EM}}}{\partial x}\Omega\right] \qquad [4.4]$$

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where:

$n$ is the atomic density,
$D_{\text{eff}}$ is the effective diffusion coefficient,
$k$ is the Boltzmann's constant,
$T$ is the absolute temperature,
$Z^*$ is the effective valency of the diffusing species,
$e$ is the electron charge,
$j$ is the current density,
$\rho$ is the electrical resistivity of the conductor line,
$\Omega$ is the atomic volume,
$\partial\sigma_{\text{EM}}/\partial x$ is the EM-induced stress gradient along the length of the conductor line, and
$b$ is a stress state-dependent coefficient, with $b = 2/3$ if $\sigma_{\text{EM}}$ is the equi-biaxial stress and $b = 1$ if $\sigma_{\text{EM}}$ is the hydrostatic stress.[11]

For a conductor line with flux blocking boundaries at both ends and embedded in dielectric material, Blech proposed that there is a critical current density $j_c$,[17] and for currents below $j_c$, that a stress gradient develops and eventually counterbalances the electron wind force, that the net atom flux then becomes zero, and that a linear stress gradient then extends over the full length of the conductor line. The effective valency $Z^*$ can be determined from the steady-state stress gradient ($\partial\sigma_{\text{EM}}/\partial x$) measured for a current density $j$ below $j_c$.

### 4.3.2 Role of passivation layers on the EM-induced strains

For insulation, antioxidation and dielectric purposes, dielectric materials and passivation layers are required in the interconnect technology. These passivation layers can greatly affect the strain evolution in conductor lines, because they confine the expansion or contraction of the lines. For ideal rigid confinement and bulk EM, the relationship between the change in local hydrostatic stress $\mathrm{d}\sigma$ and the change in local atomic density $\mathrm{d}C/C$ resulting from the atomic flux $J$ is given by equation [4.5]:[11,17,18]

$$\mathrm{d}\sigma = -B\frac{\mathrm{d}C}{C} \qquad [4.5]$$

where $B$ is bulk modulus of the conductor line and $C$ is the number of atoms per unit volume in the conductor line. If the stress produced by the EM is equi-biaxial rather than hydrostatic, as expected for grain boundary EM in a wide, columnar film with weak vertical confinement, then $B$ in equation [4.5] is the equi-biaixal modulus of the conductor line material. If the stress is uniaxial, as expected for top surface EM with strong vertical confinement, then $B$ is the uniaxial modulus.

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The passivation layer and surrounding dielectric materials play an important role in the magnitude of EM-induced strains, in which effective bulk modulus was used to replace $B$ in equation [4.5]. Hau-Riege and Thompson[18] used the finite-element method (FEM) to study the effect of the shape of the conductor line and the mechanical properties of the surrounding dielectric materials on the effective bulk modulus. Their results showed that with stiffer dielectric and passivation materials, the effective bulk modulus is larger and thus the EM induced stresses and strains are higher.[18]

### 4.3.3 Interplay between thermal and EM-induced strains

Because EM is usually studied at higher temperature and higher current density, thermal strain and EM-induced strains are both present during studies of EM-induced strain. Joule heating caused by high current density can contribute to thermal strain during the study of EM-induced strain. When the strain evolution has reached a steady state, the strain gradient predicted by equation [4.4] is a dynamic balance of atomic flux caused by EM, by the stress gradient and by thermal relaxation. For the study of pure EM-induced strain evolution in Cu conductor lines, Cu line samples are normally held at high temperature for sufficient time to allow the thermal strain to relax before the EM and X-ray strain measurements are started.

### 4.3.4 Measurements of EM-induced strains in Cu conductor lines

The Cu conductor line samples used in these measurements are described in 4.2.1. X-ray microbeam diffraction measurements were made at the Advanced Photon Source (APS) on beamline 34-ID. The X-ray beam was focused to about 0.5 μm diameter. Two Cu lines were chosen for EM testing with current flowing during the X-ray strain measurement, and two other Cu lines were chosen as control lines without current flowing, to compare with the EM test lines with the same fabrication and thermal history. The EM lines were stressed with a dc current of 2 mA, corresponding to a current density of $2.2 \times 10^5$ A cm$^{-2}$, and at a temperature of 270 °C.

Only deviatoric strains in three principal directions $x$, $y$ and $z$ were studied. Strains with positive signs are tensile, and strains with negative signs are compressive. A larger area than the Cu conductor line was scanned to make sure that all parts of the Cu lines were measured, as shown in Fig. 4.6. The total scan for the entire line took about 3 h. After each strain mapping of an EM line was completed, strain mapping of a control line was immediately made. The first measurement started after current has been flowing for 72 h in the EM-1 line at 270 °C and was completed 75 h after the start of EM. The scan of control line CL-1 was started at 75 h and

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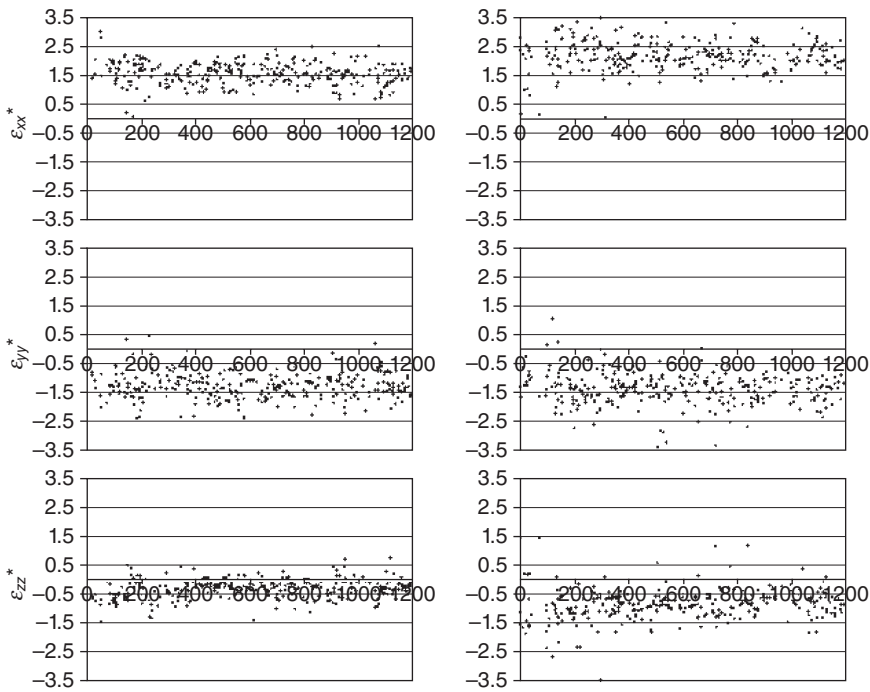
completed at 78 h. After current had been flowing in the Cu EM lines for 120 h, strain mapping in EM-2 line was started and completed at 123 h. For 123 h to 126 h, strain mapping of the control line CL-2 was carried out.

Figure 4.7 shows the strain measurement results for lines EM-2 and CL-2. No strain gradient was found in EM-2 after current had been flowing for 120 h at 270 °C. However, there was a significant drop in the average strains in EM-2, compared with CL-2. Table 4.2 shows the average deviatoric strains in the $x$, $y$, $z$ directions for the EM-1, CL-1, EM-2 and CL-2. From Fig. 4.7, the range of the strain values is also narrower in EM-2 compared with CL-2. The root mean square (RMS) variations of the strains for EM lines and for control lines are compared in Table 4.3. The flowing current significantly lowered the RMS values of the strains, making the strain distribution more uniform in the EM lines.




*4.7* Left: Deviatoric strains in EM-2 line after 120 h of current stressing at 270 °C. Right: Line CL-2 after 123 h at 270 °C. The unit of strain is $10^{-3}$. The horizontal axis of the figure shows the X-ray measurement sequence, which is the same as the distance along the Cu line, with electron flowing from right to left side.[10] (Copyright © 2010 Materials Research Society. Reprinted with the permission of Cambridge University Press.)

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*Table 4.2* Average deviatoric strains in EM lines and Cu control lines. The unit of strain is $10^{-3}$

| Average deviatoric strain | $\varepsilon^*_{xx}$ | $\varepsilon^*_{yy}$ | $\varepsilon^*_{zz}$ |
|---|---|---|---|
| EM-1 (72–75 hours) | 1.683 | −1.293 | −0.393 |
| CL-1 (75–78 hours) | 2.350 | −1.365 | −0.985 |
| EM-2 (120–123 hours) | 1.567 | −1.283 | −0.284 |
| CL-2 (123–126 hours) | 2.141 | −1.327 | −0.814 |

*Table 4.3* Root mean square (RMS) deviations of the deviatoric strains in EM lines and control lines, in units of $10^{-3}$

| RMS | $\varepsilon^*_{xx}$ | $\varepsilon^*_{yy}$ | $\varepsilon^*_{yy}$ |
|---|---|---|---|
| EM-1 (72–75 h) | 0.368 | 0.447 | 0.357 |
| CL-1 (75–78 h) | 0.498 | 0.538 | 0.519 |
| EM-2 (120–123 h) | 0.373 | 0.442 | 0.338 |
| CL-2 (123–126 h) | 0.413 | 0.501 | 0.408 |

Because there is current flowing in the EM lines, the magnitude of Joule heating needs to be estimated, to determine whether greater strain relaxation in the EM lines may be simply a thermal effect. To estimate the temperature of the EM lines with the current density used in the EM study, the resistance of the EM lines was first measured at different temperatures using very small currents with negligible Joule heating, as shown in Fig. 4.8. The resistance of the Cu lines stabilized at 14.43 ohms when the current density was the same as the EM study. By fitting the curve in Fig. 4.8, the actual temperature of the Cu line during EM was estimated to be 272 °C. Without Joule heating, the temperature of the control lines should be the same as the heating stage temperature of 270 °C. The temperature difference of 2 °C between the EM lines and the control lines could not result in the strain relaxation, because the Cu diffusion coefficient changes insignificantly between 270 and 272 °C. Therefore, we conclude that EM is the dominant cause of the strain relaxation and strain homogenization observed in the Cu EM lines.

### 4.3.5 Comparison of strain evolution for Al and Cu conductor lines

Strain evolution in Al conductor line with passivation layers has been reported by Wang *et al.*[11] and Zhang *et al.*[15] Both found that strain gradients formed during EM in the Al conductor lines. However, strain gradients along Cu conductor lines expected to develop during EM were not observed

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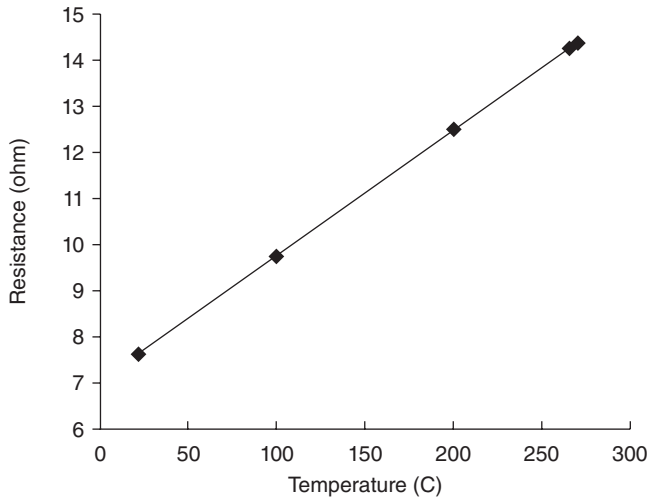


*4.8* Resistance of Cu line at various temperatures, tested at low current with insignificant Joule heating.[10] (Copyright © 2010 Materials Research Society. Reprinted with the permission of Cambridge University Press.)

in direct strain measurements. Different mechanisms have been proposed for EM in Al and Cu conductor lines. In wide Al lines, the atomic diffusion path during EM is believed to be along the grain boundaries,[11,15] whereas in Cu, surface diffusion is the main diffusion path during EM.[19] However, microstructure and line geometry are found to affect the EM mechanism. Mixture of grain boundary diffusion and surface diffusion are present in wide Cu conductor lines (more than 1 μm) with polycrystalline microstructure and surface diffusion dominates in narrower Cu conductor lines (less than 1 μm) with bamboo structures.[20] Differences in the mechanical properties, as well as differences in electrical and thermal properties, between Al and Cu make the study of EM-induced strains in Cu materials more complicated than Al. For Cu there are many factors that could affect the strain evolution during EM, which need to be systematically studied. These factors include current density, temperature, grain structure, line geometry, and mechanical properties of the dielectric, liner and passivation layer materials. In our study of strain evolution in Cu conductor lines, although the current had been flowing in the EM lines for more than 120 h, the EM may be still at the early stage, which may explain why no strain gradient had yet formed along the line. Another possibility is that the current density used in this study may not have been high enough to produce a significant strain gradient, although it was sufficient for the electrons to interact with highly strained areas in the Cu lines to cause strain relaxation and strain homogenization.

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## 4.4 Conclusions and summary

### 4.4.1 EM-induced strain relaxation in Cu conductor lines

The principles of synchrotron-based X-ray microbeam diffraction have been discussed, and results of measurements of deviatoric strains in Cu conductor lines have been described. No strain gradient was observed after EM for 120 h with a current density of $2.2 \times 10^5$ A cm$^{-2}$ at a temperature of 270 °C. However, the microbeam diffraction results show that EM has caused strain relaxation and strain homogenization in the Cu conductor lines, when compared with strain measurements in Cu conductor lines without current flowing.

### 4.4.2 Needs and opportunities for further work

Although much better EM resistance is expected in Cu interconnect materials than in Al, EM-induced failure is still one of the major concerns for the reliability of Cu-based IC devices. Because of the very different physical, mechanical, thermal and electrical properties between Cu and Al, strain caused by EM in Cu conductor lines cannot be simply understood or predicted based on the large amount of work carried out on EM behavior of Al conductor lines.

The EM mechanism in Cu conductor lines is not clearly established. The dependence of EM-induced strains on time, temperature, current density, microstructure, and mechanical properties of dielectric and passivation layer materials needs to be more systematically investigated. More reliable and efficient strain determination techniques, such as improved software to analyze the Laue patterns obtained during microbeam diffraction, are needed. Numerical modeling to explain the EM-induced strains remains challenging, as interconnect architectures become more and more complicated. Future research on the EM-induced strain and stress in Cu interconnects will provide valuable guidance for designing and fabricating more robust microelectronic devices.

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## 4.6 Appendix

To estimate the measurement uncertainty in the determination of deviatoric strains using the Laue pattern-indexing technique as described in 4.2.3, two strain-mapping measurements were made on the same Al con-

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ductor line, held at 190 °C without electromigration. Each strain mapping contained 1573 points (an area scan of 13 × 121). The measured value at each location can be considered to consist of the sum of two parts, the true strain value plus a measurement error, which is related to the measurement uncertainty. In the estimation of uncertainties, two assumptions are made:

*Assumption (1)*: At the same location, the true strain values for the two measurements are the same. The difference in results from the two measurements is caused by measurement error, related to measurements uncertainty, so

$$\begin{aligned} &\varepsilon_{1i}(\text{true}) = \varepsilon_{2i}(\text{true}) = \varepsilon_i(\text{true}) \\ &\varepsilon_{1i} = \varepsilon_i(\text{true}) + \Delta\varepsilon_{1i} \\ &\varepsilon_{2i} = \varepsilon_i(\text{true}) + \Delta\varepsilon_{2i} \end{aligned} \quad [4.6]$$

where $\varepsilon_{1i}(\text{true})$ is the true strain, $\varepsilon_{1i}$ is the measured strain, and $\Delta\varepsilon_{1i}$ is the measurement error at measurement location $i$ ($1 < i < 1573$) for the first cycle of measurements. The corresponding values for the 2nd cycle of measurements are labeled with subscript 2.

*Assumption (2)*: The average over strain measured for all measurement locations $i$ for the 1st and 2nd cycles of measurements are nearly equal, because measurement errors are random and therefore uncorrelated, thus:

$$\begin{aligned} &\langle\varepsilon_{1i}\rangle \approx \langle\varepsilon_{2i}\rangle \approx \bar{\varepsilon} \\ &\langle\Delta\varepsilon_{1i}^2\rangle \approx \langle\Delta\varepsilon_{2i}^2\rangle \approx \Delta\varepsilon^2 \end{aligned} \quad [4.7]$$

where <...> indicates averaging over all measurements.

The self-correlation function in cycle 1 is:

$$\begin{aligned} \lambda_{11} &= \langle(\varepsilon_{1i} - \bar{\varepsilon})^2\rangle \\ &= \langle(\varepsilon_{1i}^2 - 2\varepsilon_{1i}\bar{\varepsilon} + \bar{\varepsilon}^2)\rangle \\ &= \langle\varepsilon_{1i}^2\rangle - \bar{\varepsilon}^2 \end{aligned} \quad [4.8]$$

The self-correlation function in cycle 2 is:

$$\begin{aligned} \lambda_{22} &= \langle(\varepsilon_{2i} - \bar{\varepsilon})^2\rangle \\ &= \langle(\varepsilon_{2i}^2 - 2\varepsilon_{2i}\bar{\varepsilon} + \bar{\varepsilon}^2)\rangle \\ &= \langle\varepsilon_{2i}^2\rangle - \bar{\varepsilon}^2 \end{aligned} \quad [4.9]$$

The correlation function between the two measurement cycles is:

$$\begin{aligned} \lambda_{12} &= \langle(\varepsilon_{1i} - \bar{\varepsilon})(\varepsilon_{2i} - \bar{\varepsilon})\rangle \\ &= \langle(\varepsilon_{1i}\varepsilon_{2i} - \varepsilon_{1i}\bar{\varepsilon} - \varepsilon_{2i}\bar{\varepsilon} + \bar{\varepsilon}^2)\rangle \\ &= \langle(\varepsilon_{1i}\varepsilon_{2i})\rangle - \langle\varepsilon_{1i}\bar{\varepsilon}\rangle - \langle\varepsilon_{2i}\bar{\varepsilon}\rangle + \bar{\varepsilon}^2 \\ &= \langle(\varepsilon_{1i}\varepsilon_{2i})\rangle - \bar{\varepsilon}^2 - \bar{\varepsilon}^2 + \bar{\varepsilon}^2 \\ &= \langle(\varepsilon_{1i}\varepsilon_{2i})\rangle - \bar{\varepsilon}^2 \end{aligned} \quad [4.10]$$

The difference between $1/2(\lambda_{11} + \lambda_{22})$ and $\lambda_{12}$ is

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$$\begin{aligned}
&\frac{1}{2}(\lambda_{11}+\lambda_{22})-\lambda_{12}\\
&=\frac{1}{2}<\varepsilon_{1i}^2>+\frac{1}{2}<\varepsilon_{2i}^2>-<(\varepsilon_{1i}\varepsilon_{2i})>\\
&=\frac{1}{2}<(\varepsilon_i(\text{true})+\Delta\varepsilon_{1i})^2>+\frac{1}{2}<(\varepsilon_i(\text{true})+\Delta\varepsilon_{2i})^2>\\
&\quad-<(\varepsilon_i(\text{true})+\Delta\varepsilon_{1i})(\varepsilon_i(\text{true})+\Delta\varepsilon_{2i})>\\
&=\frac{1}{2}<\varepsilon_i^2(\text{true})>+\underline{<\varepsilon_i(\text{true})\Delta\varepsilon_{1i}>}+\frac{1}{2}<\Delta\varepsilon_{1i}^2>+\frac{1}{2}<\varepsilon_i^2(\text{true})>\\
&\quad+\underline{<\varepsilon_i(\text{true})\Delta\varepsilon_{2i}>}+\frac{1}{2}<\Delta\varepsilon_{2i}^2>\\
&\quad-(<\varepsilon_i(\text{true})\varepsilon_i(\text{true})>+\underline{<\varepsilon_i(\text{true})\Delta\varepsilon_{2i}>}+\underline{<\varepsilon_i(\text{true})\Delta\varepsilon_{1i}>}\\
&\quad+\underline{<\Delta\varepsilon_{1i}\Delta\varepsilon_{2i}>})
\end{aligned}\qquad [4.11]$$

Since $\Delta\varepsilon_{1i}$ and $\Delta\varepsilon_{2i}$ are both random errors, the underscored terms in equation [4.11] are zero, when the number of measurement points are large enough. Equation [4.11] can be rewritten as:

$$\begin{aligned}
&\frac{1}{2}(\lambda_{11}+\lambda_{22})-\lambda_{12}\\
&=\frac{1}{2}<\varepsilon_i^2(\text{true})>+\frac{1}{2}<\Delta\varepsilon_{1i}^2>+\frac{1}{2}<\varepsilon_i^2(\text{true})>\\
&\quad+\frac{1}{2}<\Delta\varepsilon_{2i}^2>-<\varepsilon_i^2(\text{true})>\\
&=\frac{1}{2}<\Delta\varepsilon_{1i}^2>+\frac{1}{2}<\Delta\varepsilon_{2i}^2>\\
&=\Delta\varepsilon^2
\end{aligned}\qquad [4.12]$$

As a result, the uncertainty can be estimated to be:

$$\Delta\varepsilon=\sqrt{\frac{1}{2}(\lambda_{11}+\lambda_{22})-\lambda_{12}} \qquad [4.13]$$

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# 5

# Voiding in copper interconnects during electromigration

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**Abstract**: In this chapter, the void formation mechanism in copper interconnects is discussed. The void nucleation process is described, and the differences between aluminum and copper interconnects are highlighted. The void growth mechanism is presented, emphasizing the role that the copper/cap interface plays in electromigration. Immortality in copper interconnects is discussed in the context of no-void nucleation and void growth saturation.

**Key words**: void nucleation, void growth, immortality, Blech length, copper/cap interface.

## 5.1 Introduction

Electromigration has remained a reliability issue today even though the industry started to adopt copper as an interconnect material in early 2000. Although copper is expected to be much more electromigration resistant than aluminum owing to its smaller bulk diffusivity, the different metallization scheme between the two interconnect material leads to contrasting electromigration behavior. For copper interconnects with silicon dioxide as the inter-level and intra-level dielectric, void formation leading to open-circuit failure or unacceptable resistance increase is the main reliability concern, over the possibility of short-circuit failure owing to metallic extrusion. The presence of a weak Cu/dielectric cap interface leads to a low critical stress for void nucleation, as well as a fast diffusion path. This void nucleation mechanism is discussed in detail in 5.2. Owing to the ease of formation of voids in copper, the time-to-failure in copper interconnects depends mainly on the void growth time. In 5.3, the role played by the interfaces and grain boundaries during void migration and growth is discussed, as revealed through in situ scanning electron microscopy electromigration stressing. Although electromigration leads to void nucleation and growth, it does not necessarily lead to failure. Immortality in copper interconnects is discussed in 5.4 with regards to true immortality without void nucleation and probabilistic immortality with void growth saturation. Lastly,



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the impact of scaling and introduction of new materials into the copper interconnect scheme on electromigration is briefly discussed.

## 5.2 Void nucleation

### 5.2.1 Void nucleation theory

Void formation, which begins with void nucleation and subsequent void growth, is one of the failure modes induced by electromigration in interconnects. In order to nucleate a void in an interconnect, the void nucleation location must experience a divergence in vacancy flux resulting from electromigration, and the divergence in vacancy flux must give rise to a non-equilibrium high vacancy concentration (Lloyd, 1991). Although vacancy flux divergence can occur anywhere along the length of an interconnect, let us consider the cathode end of an interconnect where a diffusion barrier is present and assume the diffusion barrier to be a perfect blocking boundary for vacancy diffusion. Under this condition, the cathode end of the interconnect experiences an electromigration-induced vacancy flux divergence and also an increase in vacancy concentration during electromigration. As electromigration progresses and eventually generates a critically high concentration of vacancy at the cathode end of the interconnect, the excess vacancies coalesce to nucleate and form a stable void. The time to nucleate a void is inversely proportional to the square of the applied current density, as shown by a model that considers both the electromigration driving force and an opposing driving force that arises from the vacancy concentration gradient (Shatzkes and Lloyd, 1986).

It must be emphasized that in order to obtain a vacancy concentration that is higher than the equilibrium vacancy concentration, the cathode end of the interconnect in the above-mentioned scenario must not have a free surface. We can assume that free surface is absent in pre-stressed damascene Cu interconnect because the interconnect is usually surrounded by a Ta-based diffusion barrier at its base and side walls, and a dielectric capping layer on the top (Fig. 5.1). In the case of Al interconnect, free Al surfaces readily oxidise to form an adherent layer of Al oxide. The effect of a free surface is such that it will act as a sink for excess vacancies that are nearby, thereby resulting in a failure to build up a non-equilibrium high vacancy concentration. This occurs during void growth and is discussed in 5.3.

If we consider that the vacancy concentration in the interconnect is in equilibrium with the hydrostatic stress acting on the interconnect (Blech and Herring, 1976), then the divergence in vacancy flux at the cathode end of the interconnect causes a tensile stress to evolve and, subsequently,

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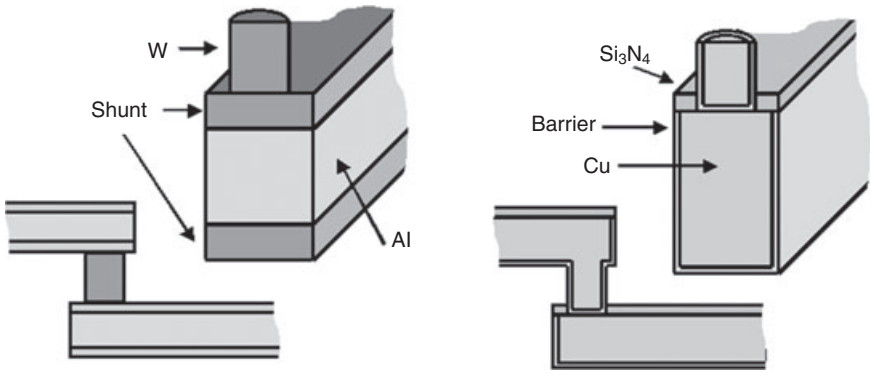


*5.1* Schematics of Al and Cu interconnect architecture. Grain boundary is the dominant diffusion path in polygranular Al interconnect whereas Cu/dielectric cap interface is the dominant diffusion path in Cu interconnect.

nucleation of a stable void occurs when a critical tensile stress is attained. The relation between vacancy concentration and hydrostatic stress is given by (Korhonen *et al.*, 1993):

$$C_{\mathrm{v}} = C_{\mathrm{v0}} \exp\left(\frac{\Omega\sigma}{kT}\right) \qquad [5.1]$$

where $C_{\mathrm{v}}$ is the vacancy concentration, $C_{\mathrm{vo}}$ is the equilibrium vacancy concentration in the absence of stress, $\Omega$ is the vacancy volume, $\sigma$ is the hydrostatic stress, $k$ is the Boltzmann constant and $T$ is the temperature. It was reported that tensile stress and compressive stress arise at the cathode and anode ends of an interconnect, respectively, during electromigration testing and the interconnect returns to a state of uniform stress after the stress current is switched off (Blech and Herring, 1976). The stress evolution within an interconnect undergoing electromigration test can be described by the following one-dimensional model (Korhonen *et al.*, 1993),

$$\frac{\partial\sigma}{\partial t} = \frac{\partial}{\partial x}\left[\frac{D_{\mathrm{eff}} B\Omega}{kT}\left(\frac{\partial\sigma}{\partial x} + \frac{Z^{*}e\rho j}{\Omega}\right)\right] \qquad [5.2]$$

where $t$ is the time, $x$ is the direction along the length of the interconnect, $D_{\mathrm{eff}}$ is the effective diffusivity of vacancy, $B$ is the effective modulus of the metal–dielectric composite, $Z^{*}$ is the effective charge number, $e$ is the fundamental charge and $\rho$ is the resistivity of the conductor, and j is the applied current density.

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### 5.2.2 Differences between aluminum and copper interconnects

Al and Cu interconnects follow different interconnect integration schemes, as shown in Fig. 5.1. Although bulk, grain boundary and interface diffusion paths are available in both Al and Cu interconnects, the dominant diffusion path in Al and Cu interconnects are grain boundary (Blech and Meieran, 1969; Rosenberg and Berenbaum, 1968) and Cu/dielectric cap interface (Hau-Riege and Thompson, 2001; Hu *et al.*, 1999), respectively. Owing to the different dominant diffusion paths, several different electromigration behaviours are observed in Al and Cu interconnects. Al interconnects have longer electromigration lifetimes when they have a bamboo-like microstructure compared with a polygranular microstructure (Cho and Thompson, 1989; Vaidya *et al.*, 1980), but the lifetimes of Cu interconnects are independent of the type of microstructure (Hau-Riege and Thompson, 2001). Longer electromigration lifetimes are observed in Al interconnects with bamboo-like microstructure because a continuous grain boundary path for diffusion along the electromigration direction is absent, and this slows down the rate of mass transport. A bamboo-like microstructure does not improve the lifetime of Cu interconnect because its dominant diffusion path is not along the grain boundary. The electromigration lifetime of Cu interconnects is found to be independent of width scaling since mass diffusion takes place along the Cu/dielectric cap interface (Hu *et al.*, 1999; Usui *et al.*, 2005).

Besides being the dominant diffusion path in Cu interconnect, the Cu/dielectric cap interface was also reported to be the preferred void nucleation site (Meier *et al.*, 1999; Hau-Riege, 2002). This resulted in Cu interconnects exhibiting longer electromigration lifetimes in via-below interconnect configuration, than in via-above interconnect configuration (Gan *et al.*, 2001; 2005), as shown in Fig. 5.2. The observation of lifetime dependence on structural configuration can be explained by the void size required to induce an electromigration failure (Fig. 5.3). For the case where the via is located below the interconnect, a void that nucleates at the Cu/dielectric cap interface is required to grow and span the entire thickness of the interconnect before the flow of electric current is obstructed. For the other case where the via is located above the interconnect, a void that nucleates at the Cu/dielectric cap interface can easily obstruct the flow of electric current even when it partially spans the thickness of the interconnect.

The critical stress for void nucleation was reported to be between 350 and 600 MPa in Al interconnects (Hau-Riege and Thompson, 2000; 2001) and ranges from less than 41 to 246 MPa (Choi *et al.*, 2009; Hau-Riege, 2002; Hau-Riege *et al.*, 2004) in Cu interconnects. It can be seen that a relatively low tensile stress is needed to nucleate a void in Cu interconnects. The relative ease of nucleating a void in Cu interconnects can also be inferred from

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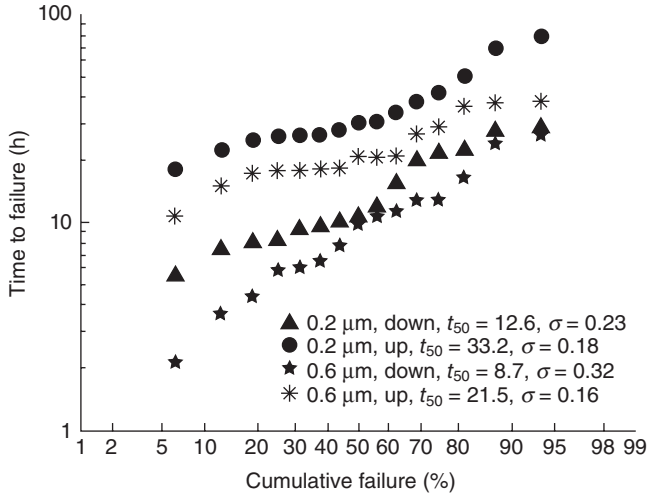
100
10
1
Time to failure (h)
1 2 5 10 20 30 40 50 60 70 80 90 95 98 99
Cumulative failure (%)
0.2 μm, down, $t_{50}$ = 12.6, $\sigma$ = 0.23
0.2 μm, up, $t_{50}$ = 33.2, $\sigma$ = 0.18
0.6 μm, down, $t_{50}$ = 8.7, $\sigma$ = 0.32
0.6 μm, up, $t_{50}$ = 21.5, $\sigma$ = 0.16

*5.2* Times-to-failure for 0.2 μm-wide and 0.6 μm-wide SiN-capped Cu interconnects in both the upstream (via-below) and downstream (via-above) test configurations. The test condition is $T = 370\,°C$ and $j = 2.0$ MA cm$^{-2}$ (Gan *et al.,* 2005).

the current density exponent of 1 that is observed experimentally (Filippi *et al.*, 2006; Hu and Rosenberg, 1999). On the other hand, the current density exponent of Al interconnects is reported to be 2. Current density exponent is a parameter in Black's model (Black, 1967):

$$t_{50} = \frac{A}{j^{n}} \exp\left(\frac{E_a}{kT}\right) \qquad [5.3]$$

where $t_{50}$ is the median time to failure, $A$ is a constant, $j$ is the current density, $n$ is the current density exponent and $E_a$ is the activation energy for diffusion. An electromigration failure process gives rise to a current density exponent of 1 if void growth is the failure rate determining step (Lloyd, 1991), whereas a current density exponent of 2 is observed if void nucleation is the failure rate determining step (Shatzkes and Lloyd, 1986). Thus, a current density exponent of 1 for Cu interconnects implies that void nucleation time is short compared with void growth time, owing to the low critical stress for void nucleation.

## 5.3 Void growth

### 5.3.1 Theory of void growth

Electromigration induces a void growth process when there is a depletion of Cu atoms at locations where there is an existing void. This requires

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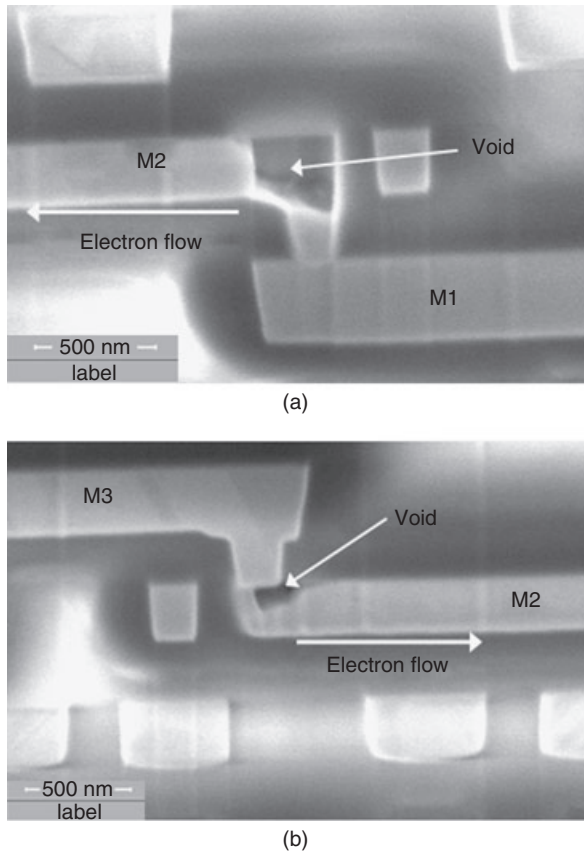


*5.3* SEM cross-section images of failed 0.2 μm-wide SiN-capped Cu interconnects in (a) downstream (via-above) and (b) upstream (via-below) configurations. A partially-spanned void is only needed in (a) to cause failure whereas a fully-spanned void is required in (b). (Gan *et al.,* 2005).

electromigration to induce a vacancy flux divergence at the location of the void. The excess of vacancies that arises from the electromigration-induced vacancy flux divergence is driven to the void, by a hydrostatic stress gradient, such that the vacancy concentration in the vicinity of the void remains close to the equilibrium vacancy concentration level. The void acts as a vacancy sink because an excess of vacancies gives rise to tensile stress, as seen from equation [5.1], while the surface of a void is stress free because the void surface is not constrained. The differences in the hydrostatic stresses therefore give rise to a driving force for the excess of vacancies in the vicinity of the void to diffuse to the void surface. The void grows larger

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as vacancies are added to it. The volume of the void increases with time as given by (Tu, 2003):

$$V = \Omega J_{EM} A t, \qquad [5.4]$$

where $V$ is the void volume, $\Omega$ is the vacancy volume, $J_{EM}$ is the vacancy flux that arises from electromigration, $A$ is the cross-sectional area of vacancy flux and $t$ is the time.

### 5.3.2 Void growth mechanisms

In situ electromigration experiments have been carried out to observe the developments in a void growth process (Meier *et al.*, 1999; Liniger *et al.*, 2002; Vairagar *et al.*, 2004b; Choi *et al.*, 2008). In unpassivated Cu interconnects, Cu grains are noticed to thin down from the top free surface to the bottom Ta-based diffusion barrier as the void grows in size (Liniger *et al.*, 2002). Grain thinning is observed to occur at the cathode end of the Cu interconnect where the presence of Ta-based diffusion barrier gives rise to flux divergence (Fig. 5.4). The occurrence of surface grain thinning is evidence that surface diffusion is the dominant diffusion path in unpassivated Cu interconnects. The same study also reported the occurrence of an edge displacement type of void growth where surface grain thinning is absent. In the edge displacement type void growth mechanism, the void is observed to start growing from the cathode end of the interconnect. A vertical interface is maintained between the void and Cu grains as the void grows, as shown in Fig. 5.5. Void growth by either surface grain thinning or edge displacement is believed to have a dependence on the local microstructure of the Cu interconnects. Grain orientation, which affects the surface energy of the void front, grain boundary orientation angle and coherency of the Cu/Ta interface, is believed to influence the void growth mechanism and void shape. This is supported by the observation of an irregular void front as shown in Fig. 5.5 after 12 h of electromigration stressing.

In addition to surface grain thinning and edge displacement void growth, voids are observed to form at a distance away from the cathode end of the Cu interconnects and subsequently drift towards the cathode in passivated Cu interconnects (Vairagar *et al.*, 2004b). Voids are seen to drift in passivated Cu interconnects because Cu surface self-diffusion has an activation energy of 0.5 eV (Hu *et al.*, 1999) which is lower than that of 0.9 eV for diffusion at the Cu/dielectric cap interface (Choi *et al.*, 2007; Usui *et al.*, 2005). It was further reported that voids are observed to grow as they drift along the Cu interconnects (Choi *et al.*, 2008). Failure occurs when the void spans the entire width and thickness of the Cu interconnects, and this may even occur before the void reaches the cathode end (Choi *et al.*, 2008).

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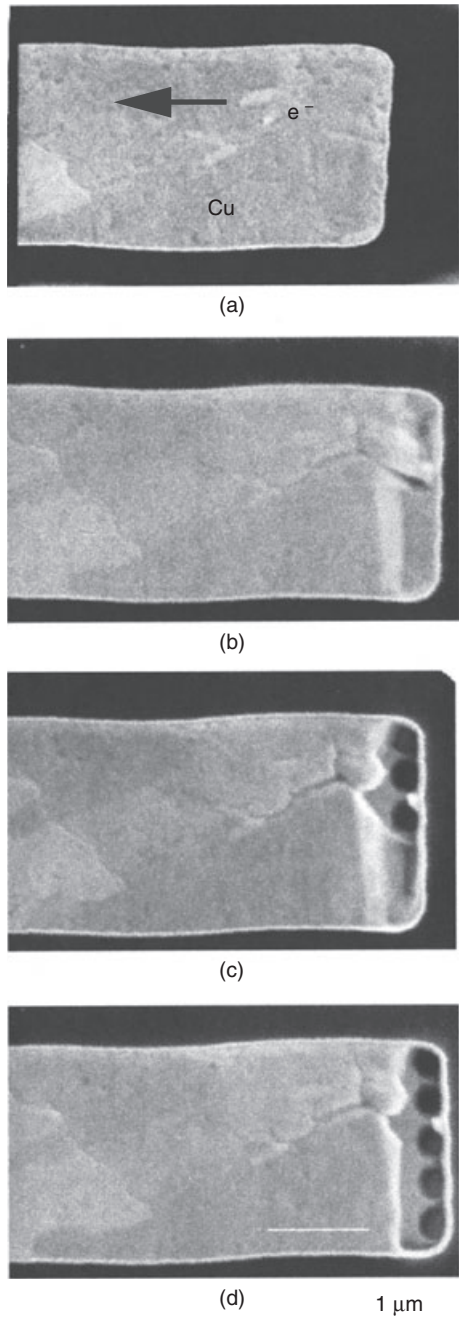


*5.4* Top view SEM images of unpassivated Cu interconnects showing surface grain thinning during void growth: (a) the beginning of the electromigration test; (b) after 2.7 h of stressing, grain thinning is visible at the cathode end of the Cu interconnect; (c) after 5.9 h of stressing, vias located at the bottom of the Cu interconnects are visible; (d) after 8.8 h of testing, all vias can be seen (Liniger *et al.*, 2002).

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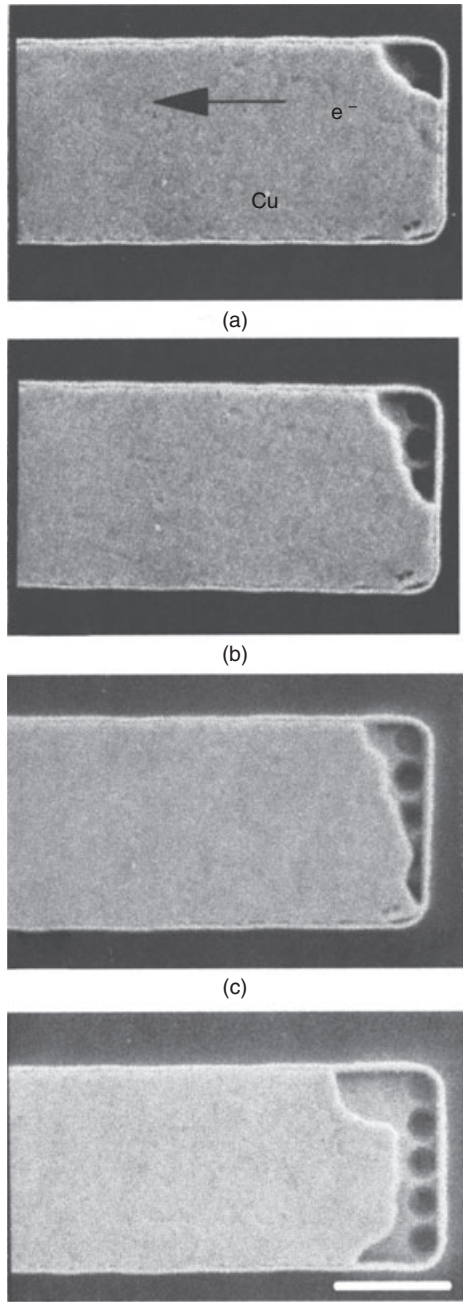


*5.5* Top view SEM images of unpassivated Cu interconnects showing edge displacement type of void growth: (a) a void formed at the corner of the Cu interconnect after 5 h of stressing; (b) a larger void is observed after 8 h and (c) after 10 h of stressing; (d) a void with irregular void front can be seen after 12 h of electromigration stress (Liniger *et al.,* 2002).

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In situ experiments on passivated interconnects observed that drifting voids can be pinned at grain boundaries, and may subsequently be de-pinned such that the voids continue to drift towards the cathode (Choi *et al.*, 2008; Vairagar *et al.*, 2004b). Energy is needed to de-pin voids that are trapped at grain boundaries, and the required magnitude of energy increases with increasing void size. It is therefore observed that large voids are unable to de-pin themselves from grain boundaries and these voids subsequently grow larger in place and give rise to failure (Choi *et al.*, 2008). On the other hand, a void continues to drift towards the cathode end of the Cu interconnect if it manages to de-pin itself from the grain boundary. The drift velocity is dependent on the applied current density and the surface diffusivity, where the surface diffusivity has been reported to vary with grain orientation (Choi *et al.*, 2007).

### 5.3.3 Effect of metal capping layer

The rate of void growth in Cu interconnects is largely determined by the mass transport at the Cu/dielectric cap interface since that is the dominant diffusion path in Cu interconnects (Hau-Riege and Thompson, 2001; Hu *et al.*, 1999). The drift velocity of Cu atoms or void front can be expressed by:

$$v_{\mathrm{d}} = \frac{D_{\mathrm{eff}}}{kT} Z^* e \rho j \qquad [5.5]$$

As Cu interconnects are surrounded by Ta-based diffusion barrier at the base and side walls, and a dielectric capping layer is deposited on the top, the effective diffusivity in the Cu interconnects is given by:

$$D_{\mathrm{eff}} = n_{\mathrm{B}} D_{\mathrm{B}} + D_{\mathrm{GB}} \left( \frac{\delta_{\mathrm{GB}}}{d} \right) + D_{\mathrm{I}} \delta_{\mathrm{I}} \left( \frac{1}{h} + \frac{2}{w} \right) + D_{\mathrm{S}} \delta_{\mathrm{S}} \left( \frac{1}{h} \right) \qquad [5.6]$$

where the subscripts B, GB, I and S refer to bulk (lattice), grain boundary, interface (i.e. Cu/Ta interface) and surface (i.e. Cu/$SiN_x$ interface) respectively; $\delta_{\mathrm{GB}}$, $\delta_{\mathrm{I}}$ and $\delta_{\mathrm{S}}$ refer to the widths of grain boundary, interface and surface, respectively; $d$ is the grain size, $h$ is the line thickness, $w$ is the line width, and $n_{\mathrm{B}}$, $(\delta_{\mathrm{GB}}/d)$, $\delta_{\mathrm{I}}(1/h + 2/w)$ and $\delta_{\mathrm{S}}(1/h)$ are the fractions of atoms diffusing through the bulk, grain boundary, interface and surface of the Cu interconnect, respectively.

Various reports have shown that longer Cu electromigration lifetime is observed when the Cu/dielectric cap interface is replaced with a Cu/metal cap interface (Gambino, 2010; Hu *et al.*, 2002). It was reported that a longer electromigration lifetime is attributed to the higher bond strength Cu/metal cap interface, which causes a reduction in the void growth rate in Cu interconnects with Cu/metal cap interface as compared to those with Cu/

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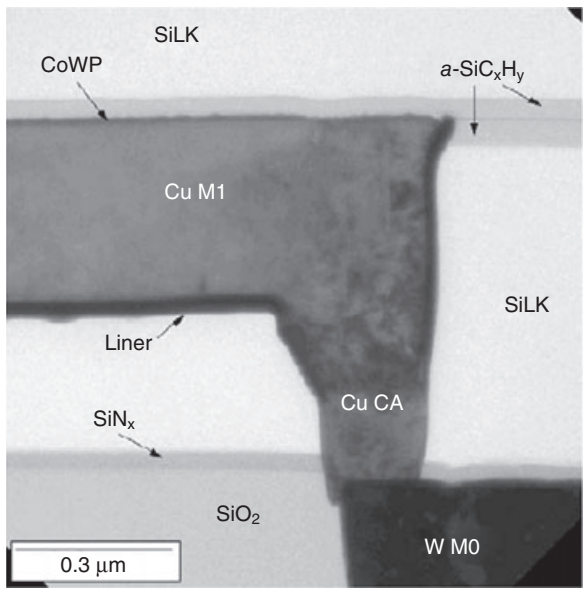
dielectric cap interface (Lloyd *et al.*, 2002). Higher adhesion energy between Cu and capping layer is shown to increase the activation energy for electromigration and, hence, reduce the rate of void growth which in turn enhances the electromigration lifetime (Lloyd *et al.*, 2002; Lane *et al.*, 2003). Hu *et al.* (2003) reported a change in the dominant diffusion path from Cu/capping layer interface to grain boundary when the top surface of Cu is coated with CoWP as shown in Fig. 5.6. When a CoWP cap is employed as the capping layer, it was further observed that Cu interconnects having bamboo-like microstructure give rise to higher electromigration lifetime than Cu interconnects with polygranular microstructure (Hu *et al.*, 2003). Activation energies of 1.0 and 1.9 eV are reported for CoWP-capped Cu interconnects with polygranular and bamboo-like microstructure, respectively (Hu *et al.*, 2003). An activation energy of 1.0 eV is similar to that of Cu grain boundary diffusion (Mishra *et al.*, 1988), whereas an activation energy of 1.9 eV is close to the reported value of 2.07 eV for Cu bulk diffusion (Peterson, 1978).

### 5.3.4 Effects of pre-existing voids in copper interconnects

Voids may exist in as-fabricated Cu interconnects (Fig. 5.7) when thermal mismatch between Cu and the surrounding dielectric materials give rise to




*5.6* TEM cross-section image of Cu interconnect coated with a CoWP capping layer (Hu *et al.*, 2003).

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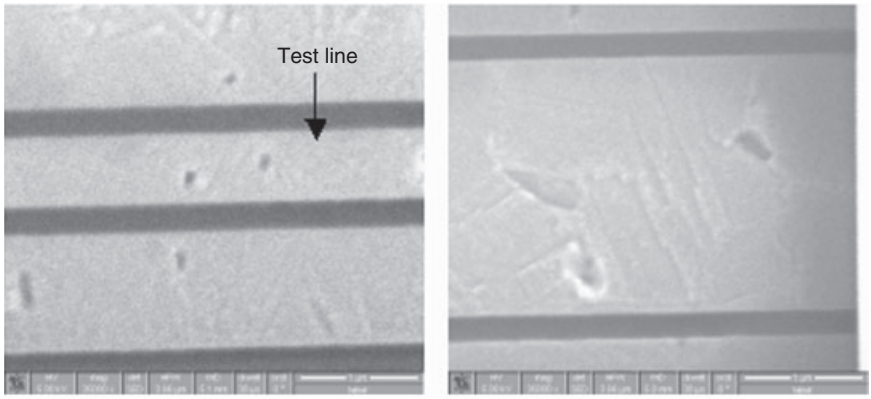


*5.7* Top view SEM images of (a) 0.61 μm and (b) 2.25 μm wide as-fabricated Cu interconnects. Microvoids can be seen at the top surface of Cu interconnects, which is at the Cu/dielectric cap interface. (Chang *et al.,* 2007).

stress-induced voiding during wafer fabrication. Pre-existing voids can significantly affect the electromigration lifetime because these voids can shorten the time to achieve a fatal void size. The size and number of pre-existing voids per unit surface area was reported to increase with increasing interconnect width, hence resulting in an electromigration lifetime that deteriorates with increasing interconnect width (Chang *et al.*, 2007).

Although electromigration physics and experiments have shown that the lifetimes of Cu interconnects without pre-existing voids are independent of the interconnect width (Hu *et al.*, 1999; Usui *et al.*, 2005), the existence of these voids can lead to an erroneous lifetime prediction when the interconnect width is scaled. In addition, voids can drift towards the cathode, grow larger in size when drifting or when pinned at grain boundary, and coalesce with other voids (Choi *et al.*, 2008; Meier *et al.*, 1999; Meyer *et al.*, 2002; Vairagar *et al.*, 2004a). Therefore, the size and initial location of pre-existing voids and their subsequent motion increases the uncertainty of reliability prediction.

It was further suggested that voids located at a distance away from the cathode end of Cu interconnects, as observed in post-electromigration failure analysis, evolved from pre-existing voids (Choi *et al.*, 2011). Simulation results showed that a pre-existing void will grow if it is within a critical distance from the cathode end of the Cu interconnect. This critical distance is inversely related to the magnitude of current density carried by the interconnect, and this inverse relation is governed by the Blech Effect (Blech, 1976) which will be discussed in detail in Section 5.4. When the pre-existing void is within a critical distance from the cathode end of the Cu

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interconnect, the Blech Effect prevents atomic flux from entering the pre-existing void from the cathode-side void front, while a continuous stream of atomic flux leaves from the anode-side void front, thereby causing the pre-existing void to grow. In the case where the pre-existing void is located along the middle of the Cu interconnect, where the Blech Effect is absent, the pre-existing void will grow if the Cu grain adjacent to the anode-side void front has higher diffusivity than the Cu grain adjacent to the cathode-side void front. These simulation results suggest that the electromigration lifetime of Cu interconnect has a stronger dependence on the applied current density and the grain diffusivity when pre-existing voids are present, and the reliability prediction of Cu interconnects is complicated by the location and size of pre-existing voids.

## 5.4 Immortality

### 5.4.1 Criteria for immortality

During electromigration, a stress gradient-induced back-stress force is induced such that the net atomic flux is given by:

$$J_a = \frac{D_{eff}C_a}{kT}\left(Z^*e\rho j + \Omega\frac{\partial\sigma}{\partial x}\right) \quad [5.7]$$

where $C_a$ is the atomic concentration, and the rest of the terms are as previously defined. A steady-state condition can occur in which the stress gradient induced back-stress force balances the electron wind force, such that the hydrostatic stress is time-invariant and linear along the line length (Blech, 1976) as illustrated in Fig. 5.8. Under this condition, the net atomic flux along the line is zero. From equation [5.7],

$$\Omega\frac{\Delta\sigma_{max}}{L} = Z^*e\rho j \quad [5.8]$$

where $L$ is the length of the line and $\Delta\sigma_{max}$ is the stress difference between the anode and the cathode.

If the critical tensile stress for void nucleation $\sigma_{nuc}$ is greater than the maximum steady-state tensile stress developed in the line, no void forms and the line does not fail, i.e. it is immortal. For the tensile stress at the cathode to be equivalent to $\sigma_{nuc}$, $\Delta\sigma_{max}$ can be expressed as:

$$\Delta\sigma_{max} = 2(\sigma_{nuc} - \sigma_0) \quad [5.9]$$

where $\sigma_0$ is the initial stress in the metal line owing to the thermal mismatch with the dielectric system.

Through the rearrangement of equation [5.8], we can derive a critical current-density line-length product $(jL)_{crit}$ that defines this condition for

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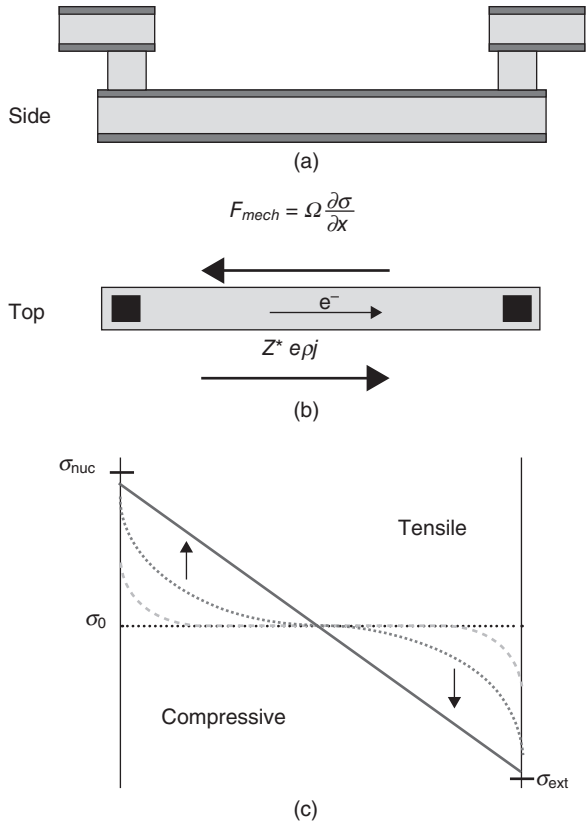


*5.8* Schematics illustrating the conditions for immortality in a straight via-to-via line without void nucleation: (a) side view and (b) top view of an interconnect with the arrows showing the direction of electron flow, electron wind force and back-stress; (c) stress as a function of location along the interconnect at different times. The line will be immortal if the maximum steady-state stresses are less than $\sigma_{nuc}$ and $\sigma_{ext}$.

immortality or commonly known as the 'Blech Effect', whereby no void nucleation occurs as:

$$jL < (jL)_{\text{crit,nuc}} \equiv \frac{2\Omega(\sigma_{\text{nuc}} - \sigma_0)}{Z^* e\rho} \qquad [5.10]$$

This means that short lines and/or lines stressed at low current densities are more likely to be immortal.

On the other hand, if $(jL)$ exceeds $(jL)_{\text{crit,nuc}}$, void nucleation occurs. However, if the void that forms in the metal line does not completely block off the current flow, it is not fatal. In Al technology, Ti-based overlayers and

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underlayers offer alternative paths for the current flow. Thus, a void can continue to grow as the current is shunted around it through the refractory metal layers, until the electron wind force and the back-stress force balance again. In this case, the line is immortal if the resistance increase associated with the void volume is lower than the maximum acceptable resistance increase $\Delta R_{max}$ and the maximum compressive stress in the line does not cause yielding or fracture of the surrounding dielectric as illustrated in Fig. 5.9. In this case, the immortality condition owing to resistance saturation is given by (Filippi *et al.*, 1995)

$$(jL)_{crit,sat} = \frac{\frac{\rho}{A}}{\frac{\rho_1}{A_1}} \frac{\Delta R_{max}}{R} \frac{2\Omega B}{Z^* e \rho} \quad [5.11]$$

where $\rho$ and $A$ are the resistivity and cross-sectional area of the high-conductivity metal, respectively, $\rho_1$ and $A_1$ are the resistivity and cross-sectional area of the shunt layer, respectively, and $R$ is the initial resistance of the line. For copper interconnects, immortality owing to resistance saturation is possible if the Ta-based liner is reliable enough to shunt the current when a void spans the whole cross-sectional area of the interconnect.

## 5.4.2 Short length effect in copper interconnects

Short length effect or immortality is only possible if the interconnect is constrained such that a back-stress force can develop to balance the electron wind force. In aluminum interconnects, immortality can be observed for a drift-type or 'Blech-type' structure, which is an unpassivated aluminum line with a more electromigration-resistant metal underlayer, owing to the formation of a self-passivating aluminum oxide. Early work on Cu drift-type structures reported a $(jL)_{crit}$ of 900–1600 A cm$^{-1}$ for a temperature range of 175–225 °C, with a transition to 225–900 A cm$^{-1}$ for an increased temperature of 250–275 °C (Frankovic and Bernstein, 1996). The decrease in $(jL)_{crit}$ at higher temperature is believed to result from a change in the yield stress of copper as $(jL)_{crit}$ is theoretically temperature independent. For Cu damascene structures, different $(jL)_{crit}$ values have been reported, depending whether it is single or dual damascene. A single damascene structure is constrained by its surrounding liner and dielectric, whereas a dual damascene structure has vias connected at the ends. Study of short length effects using dual damascene Cu structures complicates the analysis because of the possibility of voids forming in the vias, leading to early failures (Ogawa *et al.*, 2001). However, these early failures are more probably caused by processing issues, such as the weakness of the Ta liner, that lead to a reduced back-stress effect.

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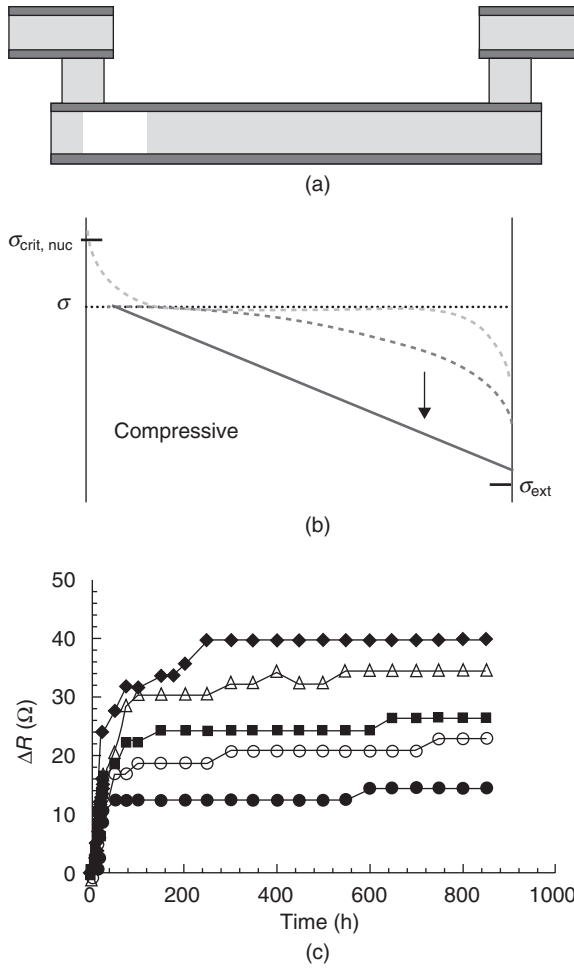


*5.9* Schematics illustrating the conditions for immortality in straight via-to-via lines with void nucleation: (a) side view of an interconnect; (b) Stress as a function of location along the interconnect at different times. (c) Experimentally reported observations of resistance saturation in Al interconnects, reproduced from (Filippi *et al.*, 1995). The line will be immortal if the maximum resistance increase is less than the specified failure criterion.

In mature interconnect technology, $(jL)_{crit}$ depends not on whether it is a single damascene or dual damascene structure, but on the location of the via at the cathode end of the test line. For a via-above (at the cathode side of the test line) structure, true immortality requires that the condition for void nucleation is not reached, as a small void that forms directly below the via can completely block electron current flow because the dielectric cap

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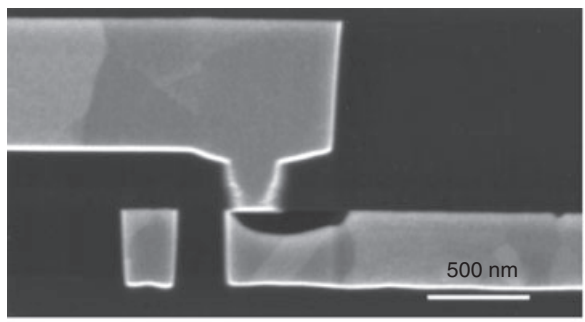
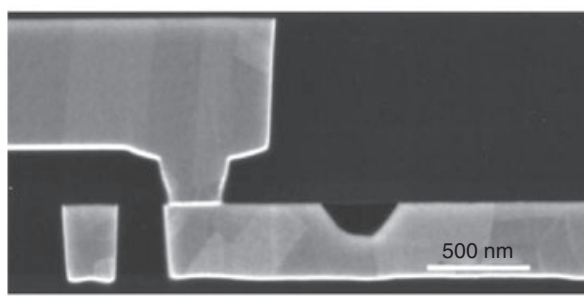
does not shunt current. On the other hand, in a via-below structure, true immortality only requires that the void at the Cu/dielectric cap interface does not grow to become full spanning across the width and height of the interconnect. Thus, the reported lower $(jL)_{crit}$ value of 1500 A cm$^{-1}$ by Hau-Riege *et al.* (2004) corresponds to the equivalent $(jL)_{crit,nuc}$ in Cu lines, as expressed in equation [5.10], because a via-above structure was used in their experiments. On the other hand, Lee *et al.* (2001) used a via-above structure and obtained a larger value of 3700 A cm$^{-1}$, corresponding to the equivalent $(jL)_{crit,sat}$ in Cu lines as expressed in equation [5.11].

Another short length study on Cu interconnect with $SiO_2$ intra-level dielectric had reported a $(jL)_{crit,nuc} < 2100$ A cm$^{-1}$ (Hau-Riege, 2002), with a probabilistic characteristic of immortality. This means that at a $(jL)$ of 2100 A cm$^{-1}$, 100% immortality was not observed in the via-above structure. Failure analysis revealed the presence of voids in all stressed samples, but the location varied (Fig. 5.10). If the void was directly below the via, an open-circuit failure was observed. However, if the void was a distance away




(a)




(b)

*5.10* SEM cross-section image of a void formed (a) directly below a via that caused an open-circuit failure and (b) at a distance away from the cathode end of a Cu interconnect which remains immortal. (Hau-Riege, 2002).

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from the via, no resistance change was detected. This observation can be explained by noting that a $(jL)$ of 2100 A cm$^{-1}$ is between $(jL)_{\text{crit,nuc}}$ and $(jL)_{\text{crit,sat}}$. Thus, a void always forms but saturates, under this stress condition. Depending on its location, this partial spanning void only causes an open-circuit failure if it is located directly below the via that cuts off the current flow.

## 5.5 Future trends

### 5.5.1 Shrinkage in interconnect dimension

As interconnect dimensions continue to shrink in accordance with Moore's law, electromigration failures owing to voiding are exacerbated. This is because the critical void volume to cause an open-circuit failure or significant increase in resistance decreases with the cross-sectional area of the interconnect. As a result, a lower amount of mass transport of Cu atoms is needed to cause a failure, thus shortening the electromigration lifetime. To mitigate this problem, a different metallic cap material such as CoWP may be required (Gambino *et al.*, 2006), that not only reduces the drift velocity along the Cu/cap interface, but also provides a current shunt for via-above structures.

Improvements in interconnect layout and design may also delay the onset of electromigration failure. Having a line extension beyond the via at the cathode end of the interconnect creates an extra volume of copper to be depleted without impacting on the resistance of the line as shown schematically in Fig. 5.11 (Shao *et al.*, 2004). This line extension, commonly known as the reservoir, delays the onset of failure. On the other hand, extra vias can be designed at the cathode as well (Girault *et al.*, 2008). The effect is similar to having a reservoir that stretches from the end of the line to the first via, as it increases the void volume required to disconnect the current path from the vias to the line.

### 5.5.2 Low-*k* dielectrics

The void formation mechanism in copper interconnects is the main reliability concern with silicon dioxide as the inter-level and intra-level dielectric. As new dielectric materials with lower dielectric constant (low-*k*) are introduced to improve the interconnect delay performance, the void nucleation and growth processes will change (Hau-Riege, 2004). New processes for the low-*k* dielectric and new dielectric cap material will lead to a decrease in the critical stress for void nucleation, which is known to be very sensitive to process variation. The weakening of the Cu/dielectric cap interface will also increase the mass transport rate, thus shortening electromigration

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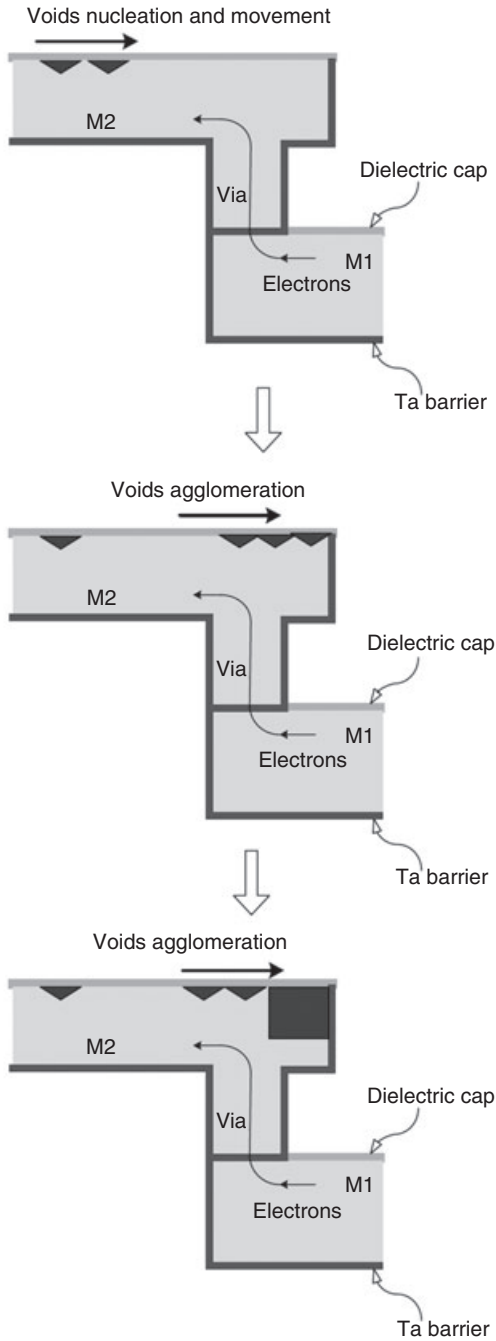


*5.11* Schematic showing the effects of having a reservoir at the cathode end, whereby voids can accumulate without impacting the line resistance. (Shao *et al.*, 2004).

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lifetime. Moreover, low-*k* materials have low bulk modulus, which delays the build-up of back-stress and thus decreases the possibility of immortality. This lower bulk modulus also increases the likelihood of extrusion failures.

## 5.6 Acknowledgements

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# 6

# The evolution of microstructure in copper interconnects during electromigration

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**Abstract**: The key concepts and experimental techniques in investigating the evolution of microstructure in Cu interconnects during electromigration are discussed and some of the fundamental changes in the microstructure during electromigration are described. The practical implications of such microstructural changes in relation to electromigration degradation mechanisms and lifetime measurement methodology are assessed.

**Key words**: electromigration, microstructure, plastic deformation, synchrotron X-ray microdiffraction, copper interconnects.

## 6.1 Introduction

Studies of the evolution of microstructure during electromigration in metallic interconnects and especially the dependence on geometries, materials and fabrication methodologies of the interconnect schemes are of the utmost importance not only technologically but also scientifically for two related reasons. First, how the microstructure evolves during electromigration can provide insights into the fundamental understanding of materials degradation mechanisms that would not otherwise be revealed by *ex situ* observations (Chen *et al*., 2007; D'Haen *et al*., 1999; Tong *et al*., 2009). Such understanding is crucial in order to control electromigration damage and thus, to a large extent, the reliability of the metallic interconnects.

Second, the current and future technological drive to smaller and smaller dimensions in the advanced interconnect schemes (Ho *et al*., 2010; McPherson, 2001) and even across to the whole new dimension completely as in three-dimensional (3D) interconnects (Lu *et al*., 2009; Saraswat, 2010) and the introduction of novel materials and fabrication processes at unprecedented rates have led us into uncharted territories in terms of scientific understanding and could very well lead to new reliability phenomena (McPherson, 2006). Studying how the microstructure evolves during electromigration in these new regimes of materials in which the length scales are near or in the order of their microstructural features (such as grain boundary, twin boundary, dislocation sub-structure, dislocation confinements) is critical if we are to control these new failure mechanisms and



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reliability phenomena. Plastic behavior in nanoscale metallic materials has already been found to deviate starkly from the classical mechanics of large-scale metallic materials (Budiman *et al*., 2008; 2011; Feng *et al*., 2008; Lee *et al*., 2010; Nix *et al*., 2007). Plasticity, in particular, thus has a significant role in the evolution of microstructure in the nanoscale metallic interconnect schemes during any thermal/electrical/mechanical loading of the materials and is therefore the subject of much of this chapter.

In 6.2, the experimental observations of the evolution of microstructure in Cu interconnects during electromigration are discussed, in particular the role that plasticity plays. Particular materials characterization techniques that enable these *in situ* observations are described. Section 6.3 covers the particular effects of fabrication processes and initial microstructure of the copper interconnect materials on its evolution and the following degradation mechanisms during electromigration especially in its accelerated or test conditions. In 6.4, the implications of these effects on the reliability of current and future generations of advanced copper interconnect schemes are discussed.

## 6.2 Copper microstructure evolution during electromigration

Metal thin films patterned into submicrometer and even nanometer-scale conductor lines comprise the communication network of all integrated circuits. When the electrical current density running through these increasingly smaller and smaller wires becomes large enough (MA $cm^{-2}$), atoms start to migrate, causing voids and hillocks to form under certain circumstances and eventually resulting in the final catastrophic failure of the device. Valek *et al.* (2002; 2003) first discovered a very unusual mode of plastic deformation occurring at an early stage of electromigration in Al interconnects. The deformation geometry introduces dislocation lines predominantly in the direction of electron flow, and thus may provide additional easy paths for the transport of point defects. Because these findings occur long before any observable voids or hillocks are formed, they may have a direct bearing on the final catastrophic events of failure of the device.

Valek *et al.* (2002; 2003) showed the unique and powerful capability of synchrotron X-ray microdiffraction. Utilizing a submicrometer-focused polychromatic synchrotron X-ray beam developed in the Beamline 7.3.3 (now Beamline 12.3.2) at the Advanced Light Source (ALS), Berkeley Lab, the technique proved advantageous as a local probe of mechanical behaviors, and in particular plastic deformation in small-scale devices. Furthermore, with this facility, *in situ* electromigration experiments can now be conducted, which are almost impossible with other characterization techniques. This capability enables us to investigate the evolution of the structure

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of the crystals as they deform owing to the enormous wind force of electrons moving from one end of the interconnect line to the other. This is an important piece of information for the fundamental understanding of electromigration degradation processes in metallic interconnects.

### 6.2.1 Synchrotron-based scanning X-ray submicron diffraction (μSXRD)

Synchrotron-based scanning X-ray submicron diffraction, also known as μSXRD (Budiman, 2008; Tamura *et al.*, 2003; Valek *et al.*, 2003), is essentially an X-ray diffraction (XRD) technique. Its unique feature stems from the fact that the X-ray beam comes from a synchrotron source, which is orders of magnitude brighter than a laboratory X-ray source, and which can be focused into a submicrometer spot size (Tamura *et al.*, 2003). This capability enables characterization of materials and their mechanical properties at high (submicrometer) spatial resolution. The polychromatic characteristic of the synchrotron radiation makes it sensitive to local lattice curvature or rotation in the crystals under consideration (Budiman, 2008).

Traditional X-ray diffraction is a technique that has been used for almost a century for elucidating the structure of materials on the macroscopic scales (0.1–10 mm). As modern electronics, photonics and even biological devices are increasingly made on a smaller and smaller scale (submicrometer and nanometer scales), a thorough understanding of the materials structure–properties–performance relationship at such length scales (0.1–10 μm) has become critical, and thus the need for high spatial resolution XRD. With the recent availability of bright third generation synchrotron sources and recent advances in X-ray focusing optics, it is now practical to develop an X-ray microdiffraction technique and apply it to characterize materials at such small scales.

The Advanced Light Source (ALS) at the Ernest Orlando Lawrence Berkeley National Laboratory in Berkeley, CA, is a third-generation synchrotron radiation source. It is well known as one of the brightest available sources of extreme ultraviolet and soft X-ray radiation in the world. A wide range of scientific activity, ranging from protein crystallography and semiconductor physics, to the pioneering technology development of the extreme ultraviolet (EUV) lithography technique critical to the continuing scaling of the microelectronics chips, have been supported by the ALS. In order to provide a wide range of energy spectra, the ALS uses a bend magnet insertion device, as well as superbend (superconducting bend magnet) sources. The X-ray microdiffraction beamline described here is located at bend magnet Beamline 7.3.3 (now Beamline 12.3.2) of the ALS. The beamline provides an extremely bright X-ray beam with a spectral range of approximately 5–20 keV.

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Because this synchrotron-based technique is what enables the *in situ* observations of the Cu microstructure evolution during electromigration, this technique is discussed in further detail in the following subsection.

*Beamline components and layout*

Figure 6.1 shows the schematic layout of the X-ray microdiffraction beamline. The X-ray beam from a bending magnet source (1.9 GeV, 400 mA, 250 μm FWHM × 40 μm FWHM, up to 3 × 0.2 mrad divergence in the horizontal and vertical, respectively) is 1:1 refocused at the entrance of the hutch by a 700 mm long platinum-coated silicon toroidal mirror operating at a grazing angle of 5.4 mrad (Tamura *et al*., 2003; Valek *et al*., 2003). Among few suitable methods for focusing high brightness white-beam X-rays, Kirkpatrick-Baez (KB) mirror pairs has been chosen for producing our X-ray focused beam in the Beamline 7.3.3 (now Beamline 12.3.2) as it is the only focusing solution to combine both achromaticity and high efficiency (Tamura *et al*., 2003). The principle of these KB mirrors has been described in detail elsewhere (MacDowell *et al*., 2001). These KB mirrors focus the X-ray synchrotron beam into a submicrometer spot size (0.5 μm × 0.5 μm FWHM). Acting as an adjustable size source for the KB demagnifying optics inside the hutch are the water-cooled tungsten slits at the entrance of the hutch. In this way spot size can be traded for flux. As white-beam has been mostly used in the studies described in the rest of this chapter, the 4-crystal monochromator in Fig. 6.1 is not utilized.

As shown in Fig. 6.1, after the X-ray white-beam is focused by the KB mirrors, there remain two main components: the sample stage, and the large area charge-coupled device (CCD) X-ray detector, both of which are mounted on a goniometer as shown in Fig. 6.2. The sample under consideration would sit on a fine XY piezoelectric stage (range of +/–50 μm), which is mounted on a coarse XYZ Huber stage (range of +/–5 mm in XY and +/–10 mm in Z) as shown in Fig. 6.3. The sample can also be mounted on a heating stage for experiments requiring temperatures up to 600 °C.

The diffraction patterns are collected with a MAR133 X-ray CCD (active area of 133 mm × 133 mm). The sample is usually mounted in a 45° reflective geometry as illustrated in Fig. 6.3, with the CCD detector on a vertical slide at a distance of approximately 50 mm from the sample area illuminated by the beam. This sample–CCD distance is optimized to give the maximum total number of reflections at a reasonable angular resolution. When illuminated with a white beam of 5–20 keV energy range, a (111) oriented Al grain, for example, gives a total of ~18 reflections, at an angular resolution of 0.01° (MacDowell *et al*., 2001).

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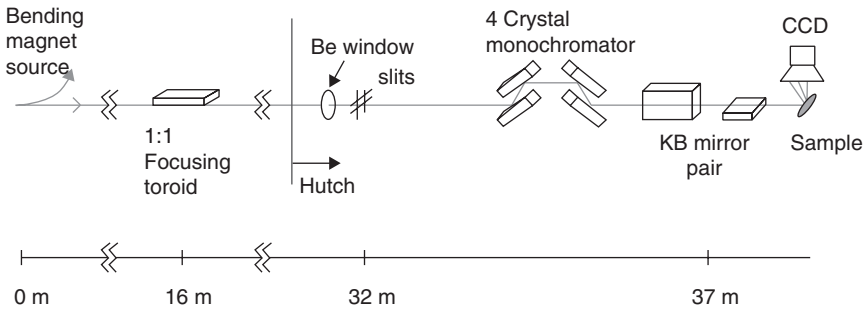
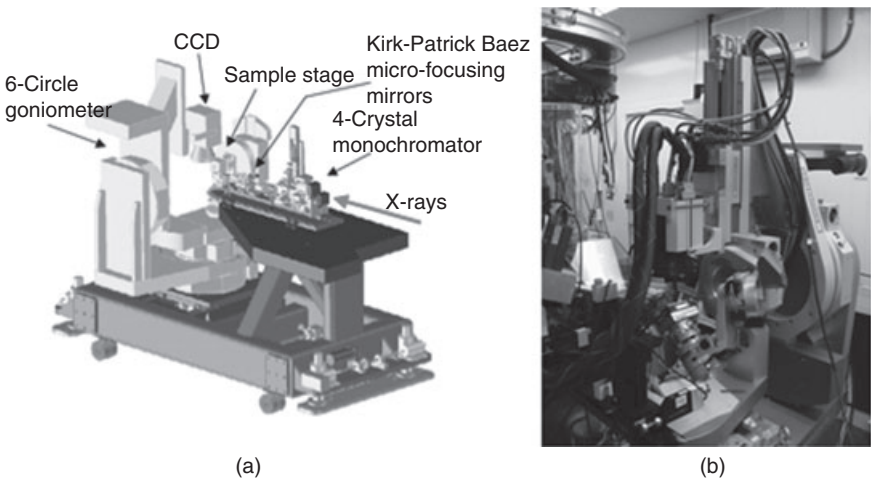



*6.1* Schematic layout of the Beamline 7.3.3 (now Beamline 12.3.2) at the Advanced Light Source (ALS), Berkeley Lab.




*6.2* Experimental endstation for Beamline 7.3.3 (now Beamline 12.3.2) at the ALS: (a) the schematic of the engineering model, and (b) picture of the actual endstation (courtesy of Tamura *et al.*, 2003).

Compared with electron microscopy techniques, X-rays offer the advantages of characterization of buried grains under overlying cap layers and multilayered films without the need of any sample preparation/destruction. *In situ* measurement under a variety of different conditions (in air, liquid, gas, vacuum, at different temperatures and pressures) thus becomes a possibility and opens opportunities for many experimental applications. The lack of sample preparation is especially important since the sample stress state can be greatly affected by any preparation processes.

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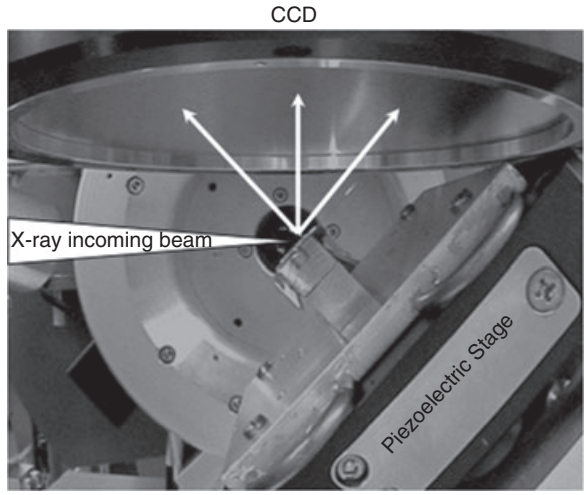


*6.3* Side view of our typical experimental setup with the two-dimensional (2D) CCD detector on top and the sample mounted in a 45° reflective geometry; X-ray incoming beam and diffracted beams are shown as white arrows, and the sample movement is precisely controlled by the piezoelectric stage.

*White-beam μSXRD as local plasticity probe*

The unique capability of the technique as a local plasticity probe stems from the polychromatic (white-beam) characteristics of the synchrotron radiation. This is what makes it sensitive with respect to local lattice curvature or rotation in the crystals under consideration. Because plasticity, especially in its special configurations in the forms of geometrically-necessary dislocations (GNDs) (Gao and Huang, 2003), is directly related to the local lattice curvature (Budiman, 2008), this technique has been most suitable for probing and studying the evolution of microstructure of materials especially in terms of its plasticity. This sensitivity to local lattice curvature is related to the continuous range of wavelengths in a white X-ray beam, allowing Bragg's Law (Bragg, 1913) to be satisfied even when the lattice is locally rotated or bent, resulting in the observation of streaked Laue spots.

White-beam Laue diffraction is a standard crystallographic method used to determine crystal orientation without rotation of the sample. Laue diffraction is usually rarely used to measure strain because the precision of most Laue instruments is low compared with modern diffractometers, and because the unit cell volume cannot be determined with a standard Laue measurement. Nevertheless, with suitable instrumentation, such as that used in the experimental setting described above, precise determination of

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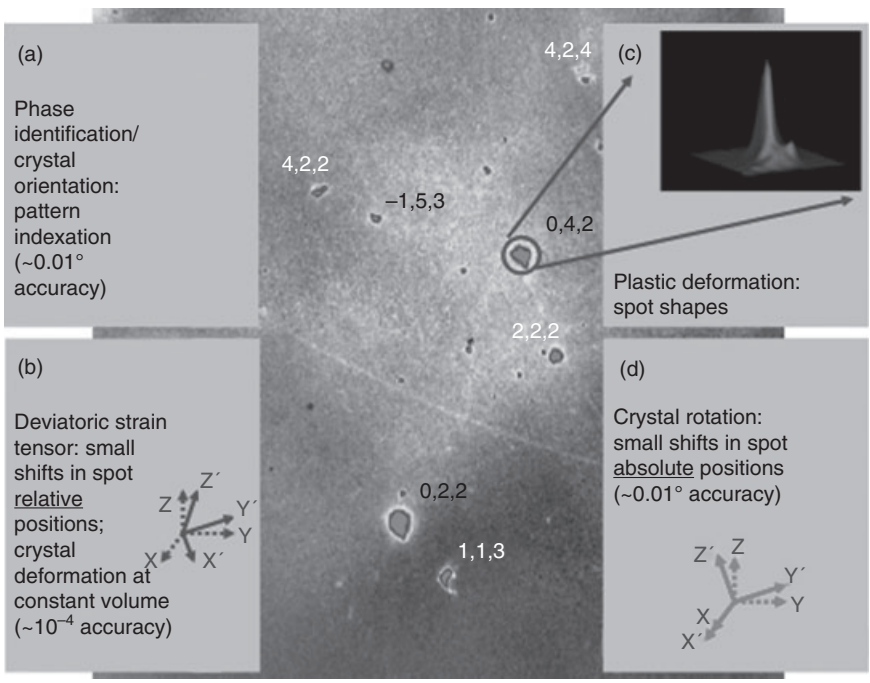
crystal orientation and distortional strain is possible. Laue diffraction might even be further extended by measuring the energy of one or more reflections to determine the full strain tensor in polycrystalline samples.

A single white-beam Laue diffraction pattern as shown in Fig. 6.4 contains a wealth of information about crystallographic orientation (Fig. 6.4a), deviatoric stresses/strains (Fig. 6.4b), and dislocation structure/density (Fig. 6.4c) as well as crystal rotation (Fig. 6.4d) in each individual crystal of the typically polycrystalline samples. Figure 6.4 shows features in a Laue diffraction pattern and the associated structural and mechanical information that they contain about the materials/sample. The shape of the Laue peak provides information about plastic deformation in the crystal (Fig. 6.4c), especially the one involving GNDs. The change in the absolute position of the Laue peak gives us the rotational deformation of the crystal body (Fig. 6.4d).

A typical X-ray microdiffraction scanning of a sample usually yields hundreds to a few thousands of these Laue diffraction patterns. Without a set of software tools that can rapidly analyze the multiple Laue patterns contained in each of the CCD images produced by our experiments, the abundant raw data could not translate to meaningful information about the




*6.4* A single white-beam CCD image consisting of multiple sets of Laue diffraction peaks from a Cu polycrystalline sample.

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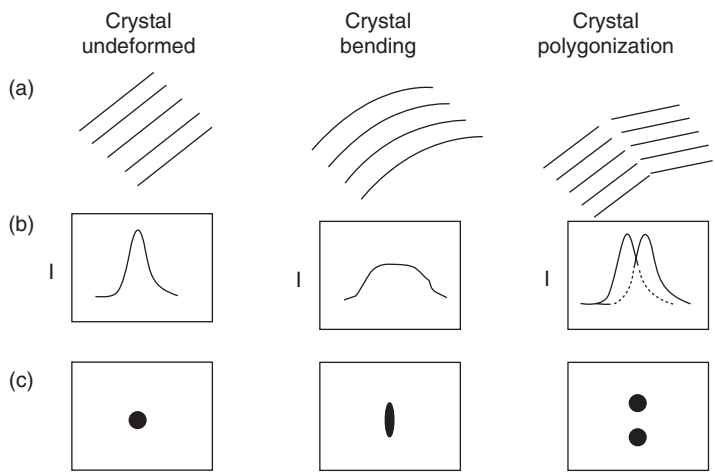
materials. A computer automated technique developed for crystallographic indexing, orientation, and strain determinations of grains in thin film samples (Chung and Ice, 1999; Ice and Larson, 2000; Tamura *et al.*, 1999; 2002) was used, and a custom-made software was developed, namely X-ray microdiffraction analysis software (XMAS) (Tamura *et al.*, 2002). It is based on an algorithm first described by Chung and Ice (1999).

*Crystal bending, polygonization and rotation*

In traditional XRD experiments, a peak at a certain angle $\theta$ means a particular (*hkl*) plane is detected, i.e. the particular angle $\theta$, interplanar distance $d_{hkl}$ and wavelength $\lambda_{Cu,k\alpha}$ (for instance) conspire such as to satisfy Bragg's Law (Bragg, 1913):

$$n\lambda_{Cu,k\alpha} = 2d_{hkt}\sin\theta \qquad [6.1]$$

Using this methodology, only elastic deformation of crystal can be determined, where strain can simply be computed from the difference of interplanar distances between atomic planes, before and after the deformation. In contrast, plastic deformation may involve curved and polygonized crystal planes, such as shown in Fig. 6.5. In such configurations, a particular crystal plane (with a fixed $d_{hkl}$ interplanar distance) may have a range of values of




*6.5* (a) Schematic diagrams of a set of crystal planes in their undeformed, bent/curved and polygonized states; (b) the expected Laue diffraction peaks corresponding to each of the crystal states; in intensity scanning over angle consisting of the Bragg angle/s; and (c) in CCD detector space (courtesy of Spolenak *et al.*, 2002).

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$\theta$ angle. This lattice curvature information is lost in traditional XRD (using a single wavelength and no tilt). However, using a white-beam X-ray, which has a range of wavelengths, Bragg's law can still be satisfied even though the $\theta$ angle varies. This means that with white-beam, a presence of lattice curvature can still be detected and even measured.

For a curved crystal plane (crystal bending), a broadened Laue diffraction peak in a certain direction is observed (Fig. 6.5) instead of a single, sharp, rounded peak typical of an undeformed crystal plane. The Laue peak broadening (also called 'peak streaking') is continuous, representing the continuum of $\theta$ values involved in the curved crystal. Crystal polygonization, in contrast, involves multiple, discreet peaks coming from slightly misoriented sub-crystal structures (such as shown in Fig. 6.5). Such polygonization often occurs following bending of the crystal where more and more dislocations pile up, and thus become unstable with respect to glide and eventually climb to form a low-angle boundary (Cahn, 1949; Gilman, 1955; Hibbard and Dunn, 1956; Patel, 1958).

This is the unique capability of our white-beam X-ray diffraction technique. Using this white-beam methodology, we can start to directly and quantitatively study the evolution of microstructure of crystalline materials especially in terms of its plasticity. This technique is especially sensitive towards crystal bending or polygonization in their simplest geometries, where a net density of parallel like-sign GNDs is formed.

Furthermore, in traditional XRD, when a body of crystal rotates, the angle $\theta$ changes and, without rotating the sample, equation [6.1] can no longer be satisfied. In contrast, using a white-beam X-ray, another wavelength is available to satisfy the diffraction condition, and thus give a constructive interference in the diffracted intensity (a Laue diffraction peak) instead on a slightly different position in the CCD camera, such as shown in Fig. 6.6. In other words, a crystal rotation would appear as a shift in the absolute positions of each of the Laue peaks belonging to the same crystal (it is to be noted that a change in the *relative* position of the Laue peaks, relative to other peaks belonging to the same crystal, in contrast, does not mean crystal rotation, but instead, shear deformation or in other words, deviatoric strains).

### 6.2.2 Electromigration-induced microstructural changes in copper interconnects

The μ-SXRD technique using focused synchrotron radiation white-beam developed in the Beamline 7.3.3 (now Beamline 12.3.2) at the ALS Berkeley Lab has been used to study the microstructural evolution at the granular level of Cu polycrystalline lines during electromigration (Budiman *et al.*,

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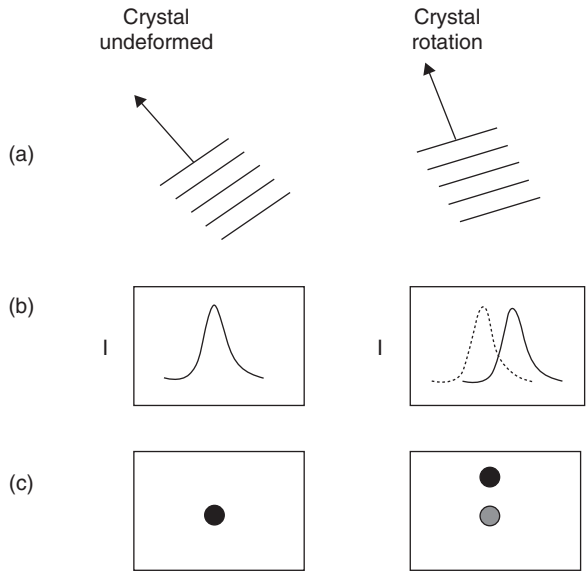


*6.6* (a) Schematic diagrams of two bodies of crystal in their undeformed/unrotated and rotated states; (b) the expected Laue diffraction peaks corresponding to each state, in intensity scanning over angle consisting of the Bragg angle (there is a shift in the absolute angular position of the peak); and (c) in CCD detector space (again, a shift in the position of the peak on the CCD detector space).

2004; 2006a; 2006b). An unexpected mode of plastic deformation was observed in damascene Cu interconnect test structures during an in situ electromigration experiment and before the onset of visible microstructural damage (such as void and hillock formation). We show here, using this synchrotron technique, that the extent of this electromigration-induced plasticity is dependent on the line width. In wide lines, plastic deformation manifests itself as grain bending and the formation of subgrain structures, whereas only grain rotation is observed in the narrower lines. This electromigration-induced plasticity tends to occur in large grains spanning across the width of the Cu lines in the form of grain bending and polygonization, whereas smaller grains tend to just rotate.

Furthermore, we observe that the bending axis of this plastic deformation coincides with one of the <112> line directions of the known slip systems for FCC crystal, and that it is always very close (within a few degrees) to the direction of the electron flow in the lines. This finding suggests a correlation of the proximity of a <112> line direction to the direction of electron flow with the occurrence of plastic behavior. This deformation geometry leads us to conclude that dislocations introduced by plastic flow lie pre-

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dominantly in the direction of electron flow and may provide additional easy paths for the transport of point defects. Because these deformations occur long before any observable voids or hillocks are formed, they may have a direct bearing on the final failure stages of electromigration.

The synchrotron technique of scanning white-beam X-ray microdiffraction in particular has enabled these *in situ* observations (Budiman *et al.*, 2004; 2006a; 2006b). Other *in situ* microstructure characterization studies have given valuable insights on the degradation mechanism of electromigration in Cu lines (Meyer *et al.*, 2002; Vairagar *et al.*, 2004; Doan *et al.*, 2000). To complement these studies, the high-brilliance synchrotron radiation used here allows *in situ* studies of crystal lattice rotation and its evolution during electromigration. This is an important piece of information that contributes to the fundamental understanding of electromigration degradation mechanisms. In the following subsection, the experimental details of the investigation will be discussed.

### *Experimental*

The interconnect test structure used here is an electroplated Cu damascene line manufactured by Intel Corporation (Budiman *et al.*, 2004; 2006a; 2006b). The test line has dimensions of 70 μm in length and approximately 1 μm in thickness, with two different widths of 1.6 and 0.6 μm. The lines are embedded in a $SiO_2$/SiOF interlayer dielectric film. The structure is then passivated with nitride and polyimide. The interconnect lines were produced by the damascene technique in which the copper is plated out into open channels and then mechanically polished to the desired thickness. Both vias at either end of the line connect to a lower metallization level, which, in turn, connects to unpassivated bond pads which are used for electrical connection. A schematic diagram of these structures with line dimensions is shown in Fig. 6.7.

The white-beam X-ray microdiffraction experiment was performed on Beamline 7.3.3 (now Beamline 12.3.2) at the Advanced Light Source, Berkeley, CA. The electromigration test was conducted first at 300 °C. Current and voltage were monitored at 10 s increments. The sample (width 1.6 μm) was scanned in 0.5 μm steps, 10 steps across the width of the line and 160 steps along the length of the line, for a total of 1600 CCD frames collected as illustrated in Fig. 6.8. A complete set of CCD frames takes about 6 to 7 h to collect. The exposure time was 4 s plus about 10 s of electronic readout time for each frame. In this manner the Laue pattern and information regarding plastic deformation for each grain in the sample was collected for each time step during the experiment. The current was ramped up to 50 mA ($j = 3.1$ MA cm$^{-2}$) over the course of 96 h, and then set at that value for the rest of the test.

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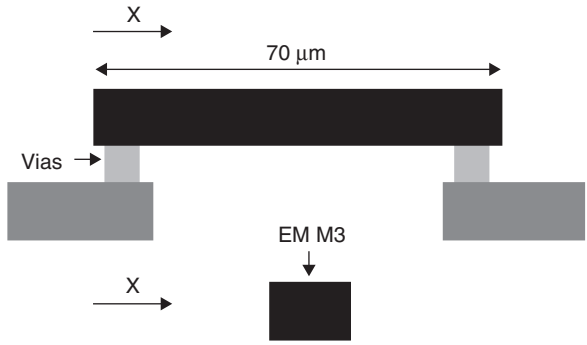
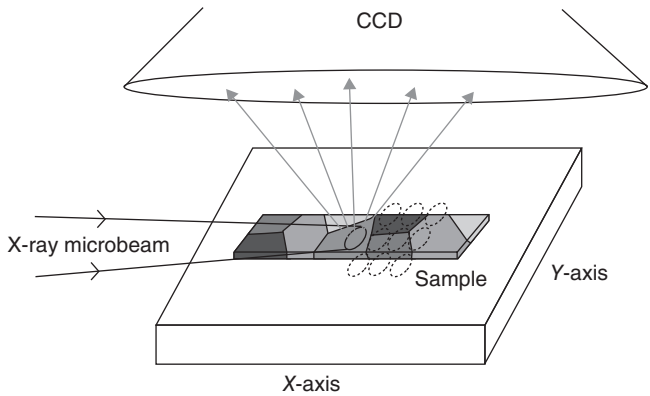



*6.7* The schematic diagram of the Cu electomigration test structures manufactured by Intel Corporation (Budiman *et al.*, 2004; 2006a; 2006b).




*6.8* Schematic diagram of a scanning white beam X-ray microdiffraction experiment. The incoming X-ray beam illuminates a volume that may consist of more than one crystal and the diffracted beams from each crystal are captured by the CCD detector placed above the sample. Laue patterns are collected from each discrete volume of the sample, followed by the next volume in a discrete-step scanning mode (courtesy of Valek, 2003).

The second group of tests was conducted at a higher temperature, 360 °C, for reasons that are discussed later in this chapter. The narrow sample (0.6 μm) was scanned in the same manner as above, except that the current ramp up was ≤20 mA ($j$ = 3.3 MA cm$^{-2}$) over the course of 96 h, and then set at that value for the rest of the test.

A rough elemental map of the sample has first to be created using scanning X-ray fluorescence, so that the region of interest can be more precisely pinpointed. For the samples in our experiments, we typically used copper,

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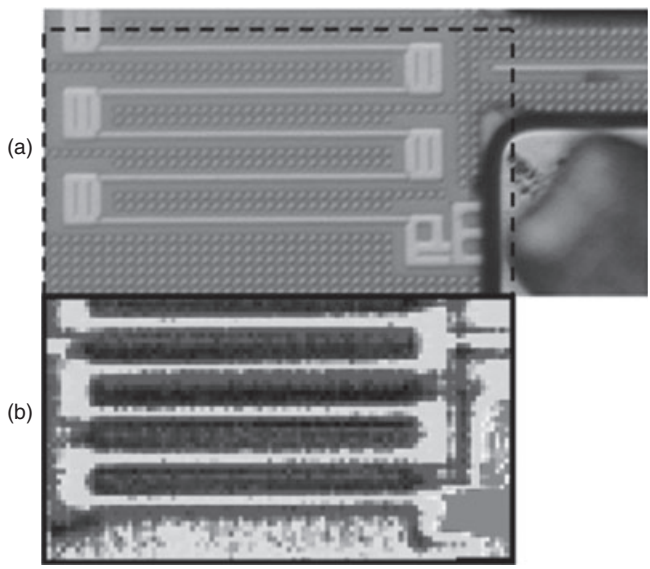
titanium, platinum and gold fluorescence signals. Subsequently, the area of interest can be precisely located by using the piezoelectric positioning stage. A typical big-picture elemental map is shown in Fig. 6.9, from which the exact co-ordinates can be determined for a more precise X-ray microdiffraction scan, and Laue patterns can thus be collected from each discrete area in the coordinates of interest.

*Initial microstructure*

We first describe the microstructure of the wide (1.6 μm) damascene Cu test structures. The grain out-of-plane and in-plane orientations in these lines as determined by white-beam X-ray microdiffraction through the passivation layer are shown in Fig. 6.10a and 6.10b, respectively.

Figure 6.10a shows all grains along the interconnect line with the <111> direction of the individual grains varying from 0° (normal to sample surface) to 54.7° away from the normal of the sample surface. In other words, the darker the color of the grains, the closer those grains are to having <111> out-of-plane orientation, and the lighter the color, the further away they




*6.9* Examples of fluorescence mapping for locating the sample's overall picture: (a) a series of horizontal copper interconnect lines (Budiman *et al.*, 2004; 2006a; 2006b) and (b) the corresponding fluorescence mapping using copper's characteristic radiation wavelength (mid-gray = high intensity of copper fluorescence characteristic radiation, light gray = medium, dark gray = low). A 0.5 μm step size in *x* and *y* was used.

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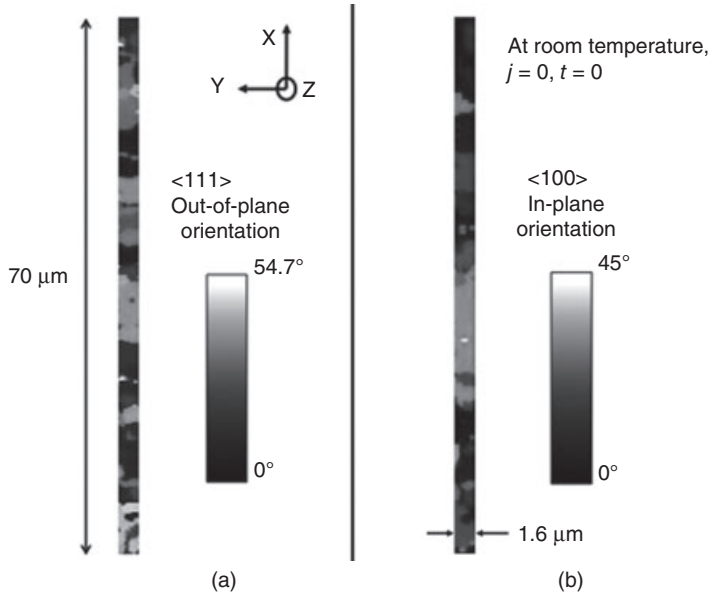


*6.10* Grain orientation mapping of the wide (1.6 μm) passivated Cu lines using synchrotron-based X-ray microdiffraction with a focused beam (FWHM ~ 0.8 μm): (a) crystal <111> out-of-plane orientation; (b) crystal <100> in-plane orientation (Budiman *et al.,* 2004; 2006a; 2006b).

are from having <111> out-of-plane orientation. It is evident from Fig. 6.10a that Cu grains in the damascene interconnect test structures were found in a wide range of out-of-plane orientations. This is consistent with observations on industry-relevant Cu interconnect test structures (Lingk *et al.*, 1999a; 1999b; 2000). Only a few of the grains (black-colored in Fig. 6.10a) are actually <111> grains, some others are quite close (dark) to being <111> grains, whereas many others are far off (light white to colored), even approaching <100>-out-of-plane-oriented grains (54.7° off).

Most of the grains are large grains spanning across the width of the line. It is reasonable to suspect that the Cu grains here extend through the whole thickness of the line, making it a bamboo structure. This is true along the line, however, in areas close to the via regions, grains are smaller, and more likely to be three-dimensional in structure (not bamboo). This trend has been reported (Besser *et al.*, 2001; Doan *et al.*, 2000; Lingk *et al.*, 1999a; 1999b; 2000), where the wider Cu damascene lines were shown to be closer to the behavior of Cu blanket films (bamboo structure), whereas the narrower lines exhibit behaviors toward three-dimensional polycrystalline structure.

Similar observations were found with the in-plane orientation. Figure 6.10b shows all grains along the interconnect line with the <100> direction of the individual grains, projected to the sample surface, varying from 0°

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(exactly lining up with the positive $x$ direction) to 45° away from $x$-axis. It may appear that the in-plane orientations of the Cu grains in this line are not too widely-ranged. However, it should be noted that as it is projected <100> direction on the sample surface, the same color in this map does not necessarily mean a single crystal/grain, but in contrast to the out-of-plane orientation mapping (Fig. 6.10a), it is evident that the same color in this map can actually be a few grains. Thus, we suspect that the Cu grains in this wide line are as varied in in-plane orientations as they are in out-of-plane orientations.

Exact grain orientation mapping of the narrow line (0.6 μm) of these Cu damascene test structures, however, proves to be difficult and rather unreliable. The X-ray spot size (0.5 μm × 0.5 μm) currently used in ALS Beamline 7.3.3 (now Beamline 12.3.2) was relatively large for the dimensions of the narrow line (0.6 μm linewidth). That makes diffraction spot indexing often very difficult and thus mapping of grain orientations and other further quantitative analyses unreliable.

*Upon electromigration loading*

Electromigration tests were conducted *in situ* on the damascene Cu test structures. Figure 6.11 shows the evolution of the Laue diffraction spots for several grains in the wide (1.6 μm) Cu line during the *in situ* electromigration experiment. If we examine the individual diffraction spots after electromigration in some detail we find that in certain grains the spots broaden not in any random direction but always in the $y$ direction across the line. The Laue diffraction spots coming from undeformed crystals are nominally rounded in shape, such as shown in Fig. 6.11 at the initial stage of the electromigration test (at $j = 0$, $t = 0$, and room temperature).

The diffraction spots have been converted to $q$-space (reciprocal space), with the $x$-axis along the length of the line, the $y$-axis across the line, and the $z$-axis normal to its surface. We find that, as the electromigration test progresses, in certain grains the spots broaden, whereas in some grains, they split into two different spots. This broadening and splitting of diffraction spots is observed not in any random direction but always along the $y$-axis in $q$-space, which is the width direction of Cu line.

Broadening of the peak is observed in a few grains that are large and span across the width of the line. Figure 6.12a–6.12c display exemplary results of such grains, Grain 2 (in the middle of the line). Here the results of digital intensity traces across the broadening direction of the Diffraction spots in the initial, mid- and end-state (after the end of the electromigration test) are shown.

Such broadening and splitting of the diffraction spots were observed in all three different wide test structure samples examined in our experiments. In each of them, a few grains (between 5 and 9) among a total of usually

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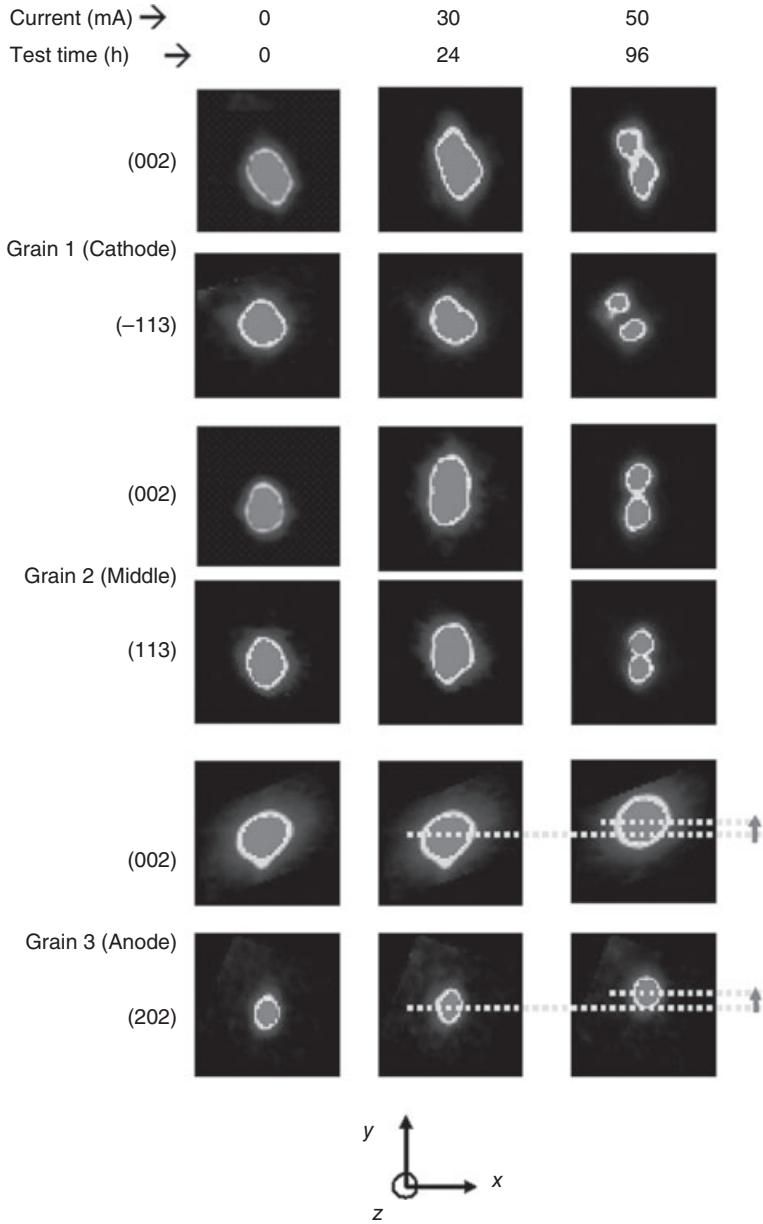


*6.11* Evolution of Laue diffraction spots (in q-space) of three grains (one at the cathode end, one in the middle, and one at the anode end of the line) during an *in situ* EM experiment (Budiman *et al.*, 2004; 2006a; 2006b). For each reflection, the area of q-space is kept constant with the length of each side of 0.03 $Å^{-1}$. Following the evolution of each spot, the reference location is kept constant.

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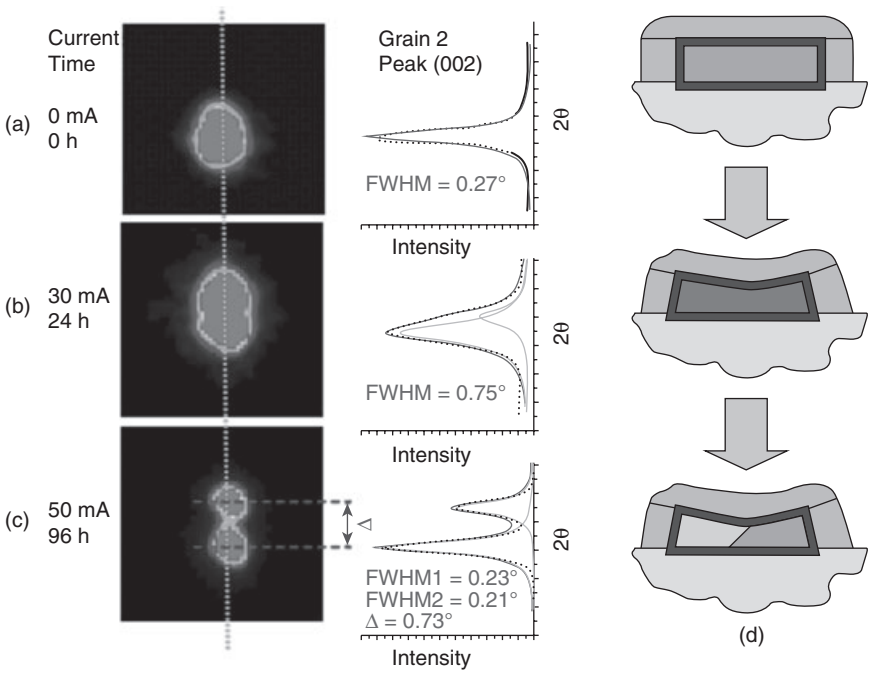
around 100 to 150 grains, were found to show this behavior after electromigration under similar test time, current and temperature.

The broadening of the diffraction spots represents crystal bending of the Cu grains in the line, whereas the split diffraction spots indicate the formation of low-angle boundary subgrain structures. From Fig. 6.12a–6.12c, it is thus evident that Grain 2 has evolved from initially, an undeformed crystal, to a plastically-bent crystal, and then lastly, to polygonized subgrain structures, such as illustrated in Fig. 6.12d. Each of the features here illustrates the corresponding Laue diffraction observations on the left side. From the amount of broadening we can calculate the bending of the Cu crystal, and from the amount of splitting, the angle of misorientation.

We can then use the broadening and the spot splitting observed to obtain information about the dislocation structure in the grain induced by electromigration. For instance, from the streak length of Fig. 6.12b as measured in




*6.12* Quantitative measurement of the evolution of a Laue diffraction spot of Grain 2 during an *in situ* EM experiment (Budiman *et al.*, 2004; 2006a; 2006b); Broadening is shown as the spot evolves from (a) to (b), and peak splitting, signifying the formation of low-angle grain boundaries, is evident in (c) as EM progresses. The evolution of Grain 2, in the cross-section of the line, is illustrated from undeformed, to plastic bending, to formation of sub-grain structures in (d).

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the CCD camera and the sample to detector distance we obtain the curvature angle of the grain of 0.75°. Because the mapping of the out-of-plane orientation of the crystal along the Cu line indicates a near bamboo structure, the grain width is about the same as the width of the line (1.6 μm), from which we get the radius of curvature of the grain, $R$ = 126 μm. The GND density to account for the curvature observed can be calculated from the Cahn–Nye relationship (Cahn, 1949; Nye, 1953), $\rho = 1/R\boldsymbol{b}$, where $\boldsymbol{b}$ is the Burgers vector. The GND density is then $\rho = 3 \times 10^9$ cm$^{-2}$. The total number of dislocations introduced is only 49.

To obtain quantitative information on polygonization walls (small angle grain boundaries) from the spot split in Fig. 6.12c we observe that the Laue spot splitting, $\Delta_\theta = 0.73°$. From this misorientation and Burgers' model of a small angle grain boundary $\Delta_\theta = \boldsymbol{b}/L$, where $L$ = dislocation spacing, we find $L$ = 212 Å which amounts to 45 dislocations in the boundary.

Similar basic observations were made by Valek *et al.* (2002; 2003) in a related prior study in Al(Cu) interconnect lines in which a very early stage of plastic deformation and microstructural evolution during an electromigration test was also detected (shown in Fig. 6.13) long before any macroscopic damage became visible, by using the same technique (Budiman, 2008; Tamura *et al.*, 2003; Valek *et al.*, 2003). In addition, it was observed that, during *in situ* electromigration, a gradient of plastic deformation evolves along the line, resulting in bending and in polygonization of the largest grains between the cathode and the anode end. Smaller grains do not readily deform but do rotate as electromigration proceeds. Plastic deformation is initiated at the cathode end and gradually progresses toward the anode end until a steady state is reached. Further quantitative analyses of these Al(Cu) results were later conducted by Kai *et al.* (2008a; 2008b) and showed a consistent trend of plasticity in Al(Cu) as in Cu interconnect lines (Budiman *et al.*, 2004; 2006a; 2006b).

### *Linewidth effects*

We now describe *in situ* electromigration studies on another damascene Cu test structure with a different linewidth (0.6 μm). The higher test temperature of this group of experiments was designed to give more pronounced streaking of the Laue peaks as the grains undergo electromigration. A previous similar electromigration study has shown an extensive broadening of peaks in the Al(Cu) system (Valek *et al.*, 2002; 2003). By increasing the test temperature of this group of experiments, we aim to have a similar homologous temperature ($T/T_M$) to that of the previous study on Al(Cu), which was ~0.51. The homologous test temperature ($T/T_M$) for the present study of narrow Cu lines was ~0.48, which is higher than the homologous temperature for the wide line experiments discussed above (~0.4).

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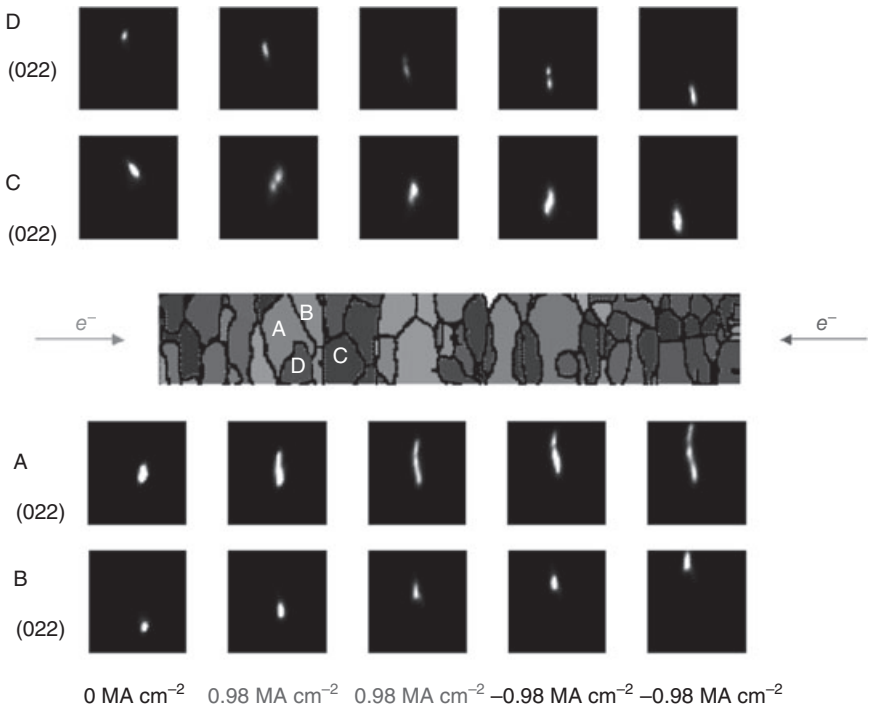


*6.13* Similar observation of the EM-induced plastic deformation in Al(Cu) interconnects (Valek *et al.*, 2002; 2003); The evolution of Laue diffraction spots from grains A, B, C and D (locations in the line are as shown in the grain mapping) from initial state to after some electromigration with reversed current directions (courtesy of Valek, 2003).

However, our observation of the peaks of the grains in the narrow Cu line (width = 0.6 μm) did not show any broadening of the peaks during electromigration. This is true despite the higher temperature used in this group of experiments. Instead, grain rotations, similar to that of Grain 3 in Fig. 6.11, are observed throughout the length of the line. The rotation of grains manifests itself as a shifting in the position of the Laue spot; from the direction and magnitude of the shift, we can calculate the axis and amount of the crystal rotation.

The narrow Cu line thus appears to behave less plastically in response to similar electromigration current density stressing than the wide (1.6 μm) line. Narrower Cu lines thus seem to have higher electromigration resistance (than the wider Cu line). The resistance to plastic flow and the reasons why only grain rotation occurs in the narrow Cu line are not well understood at present. However, a higher resistance to plastic deformation in

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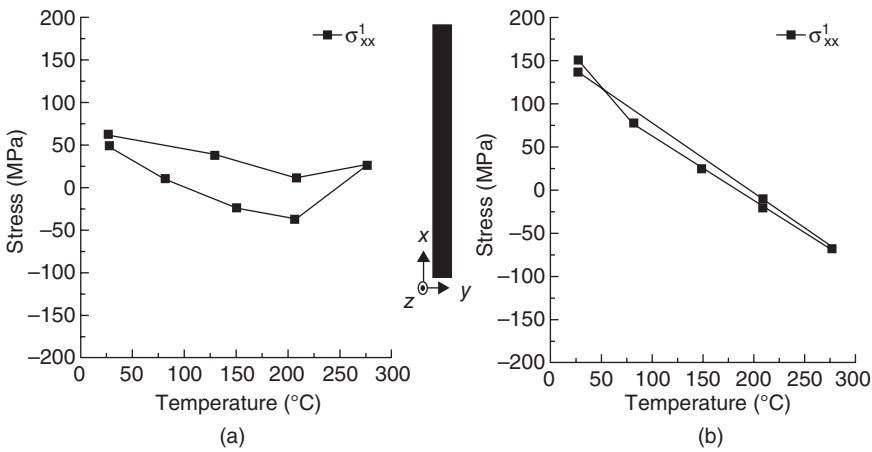
smaller structures, especially for Cu line structures, has also been reported by Spolenak *et al.* (2000; 2002).

In these studies (Spolenak *et al.*, 2000; 2002), thermal cycling of the wide Cu damascene line (5 μm) was shown to exhibit plastic deformation with yield stresses in the range 50–100 MPa in compression (Fig. 6.14). In contrast, the narrower line (0.8 μm) in that study indicated no such yield behavior and deformed only elastically over the entire temperature cycling range. These observations are consistent with our electromigration results. Streaking of X-ray Laue spots indicating plastic bending of grains is observed for the wider 1.6 μm line, but is absent for the narrower line (0.6 μm).

*Effects of in-plane orientations*

The consistent direction in which the electromigration-induced plasticity has been observed both in Al (Valek *et al.*, 2002; 2003) as well as Cu interconnect lines (Budiman *et al.*, 2004; 2006a; 2006b) was discussed earlier. Here, we further investigate the specific direction of the plastic deformation in term of electromigration current direction. We use the Laue peak streaking simulation to study the possible mechanisms of plasticity. By matching the simulation with the actual streaking pattern, we can make some conjectures as to which particular slip system, among the 12 possible slip systems known for FCC metals, might be responsible for the streaking pattern.

Coming back to the wide lines, Fig. 6.15 shows the movement of Laue spots of Grain 2 during the electromigration test, and a comparison with




*6.14* Deviatoric stress ($\sigma_{xx}'$) versus temperature graphs suggest plastic deformation in: (a) the wide (5 μm) Cu line, but not in: (b) the narrow (0.8 μm) geometry, consistent with the EM plasticity observation in Cu lines in the present study (courtesy of Spolenak *et al.,* 2002).

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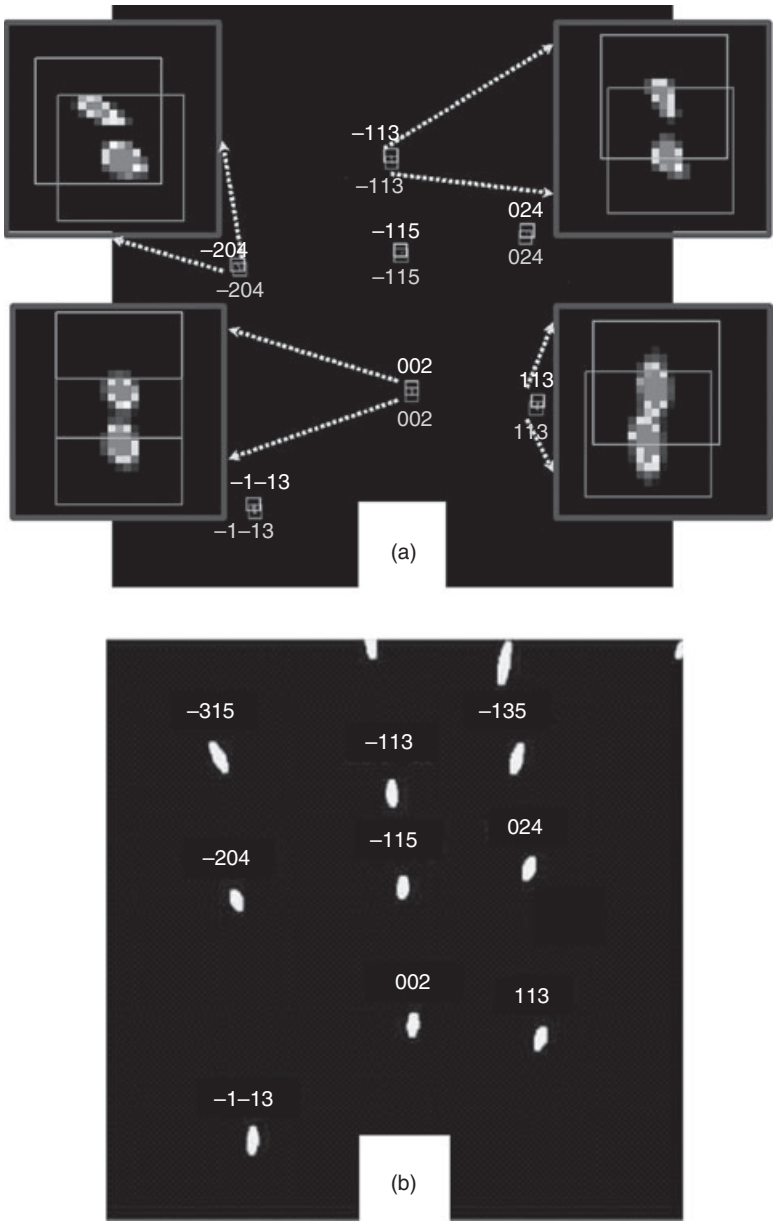


*6.15* (a) Laue reflection spots at the initial stage (lower square) and after they split into the second set of reflection spots (upper square); (b) simulation of the same initial set of reflection spots streaked based on a particular slip system showing a match with experiment (Budiman *et al.*, 2004; 2006a; 2006b).

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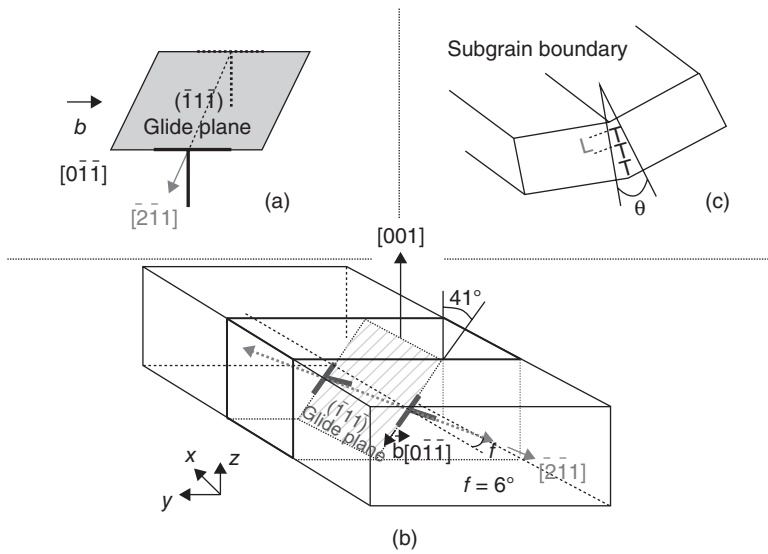
simulation result. Working within the Cahn–Nye crystal bending model (Cahn, 1949; Nye, 1953), and knowing the initial and end states of each of the diffraction spots, we can simulate the dislocation processes in the crystal necessary to cause the transformation of diffraction spots from their initial state to their final streaked/split/shifted state. We discovered that indeed the movement of the diffraction spots in Fig. 6.15a can be simulated by certain dislocation slip processes belonging to a slip system known to operate in FCC crystals (Fig. 6.15b). Figure 6.16a then describes the particular slip plane, slip direction and line direction in Grain 2 with respect to the interconnect line co-ordinates that are involved in the respective movement of diffraction spots.

Grain 2 is a large grain spanning across the cross-section of the line, and thus can be modeled as shown in Fig. 6.16b. The simulation shows one possible scenario of evolution of the grain as electromigration progresses. Point defect transport on the interfaces of the Cu line initiates the production of dislocations within the crystal of Grain 2 and activates their movement. Dislocations glide on a {111} plane that is tilted 41° from the surface of the sample. As dislocations accumulate on the glide planes, they become unstable with respect to climb and begin to coalesce into tilt dislocation




*6.16* (a) The active slip system for which the simulation predicts the movement of reflection spots correctly in Fig. 6.15a and 6.15b; (b) Modeling of slip deformation in Grain 2; (c) subgrain boundary formation through polygonization (Budiman *et al.*, 2004; 2006a; 2006b).

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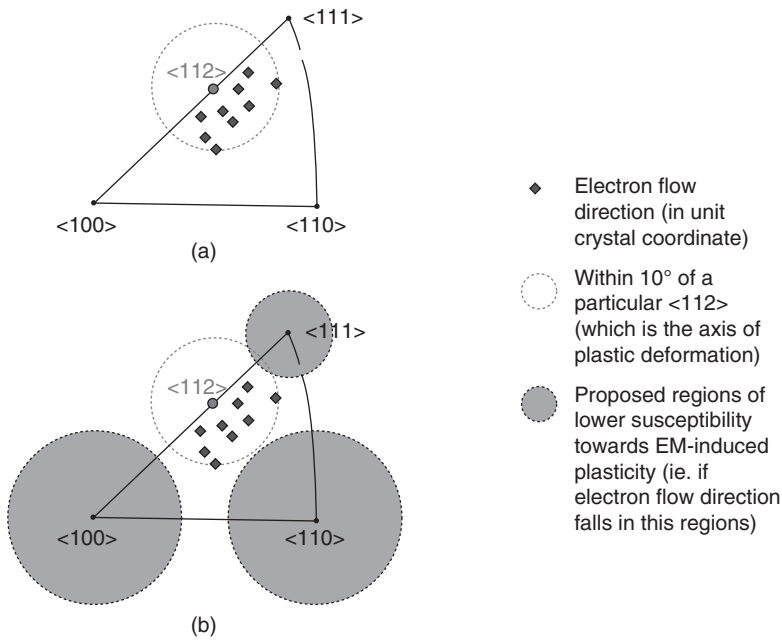
walls as illustrated in Fig. 6.16c. This series of events would manifest itself in the form of split Laue peaks following a certain direction as experimentally observed during electromigration to Grain 2 as shown in Fig. 6.15a.

We also observe that the <112> type direction for the tilt axis of the crystal is very close (within a few degrees) to the direction of the electron flow, or in other words, to the direction along the length of the line. The example in Fig. 6.16b shows a 6° deviation between the axis of tilt, which is a <112>, and the direction of electron flow. More specifically, upon further inspection, this particular <112> was also found to be the closest <112> in Grain 2 to the direction of electron flow.

Further, more complete, studies confirmed that this observation holds true for all the Cu grains in the current experiment exhibiting plastic bending and/or polygonization (formation of subgrain structures). This is shown in Fig. 6.17a. Nine large Cu grains with the observed plastic bending/




*6.17* Proximity between a particular <112> direction (which is also the axis of plastic deformation) with the direction of the electron flow in the crystal is suggested to be correlated with the occurrence of EM-induced plastic deformation: (a) nine large Cu grains (Budiman *et al.*, 2004; 2006a; 2006b) with the observed plastic bending/ polygonization are represented by the nine bullets within 10° of a particular <112> direction; (b) the shaded regions represent preferred in-plane textures proposed to give higher resistance towards EM-induced plasticity.

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polygonization are represented by the nine bullets within 10° of the closest <112> direction of their respective crystal to the direction of the electron flow. The bullets represent the direction of the in-plane crystallographic orientation of each of the respective grains in the direction of the electron flow in the line. To put it simply, all grains with a <112> direction pointing in the direction of the length of the line were observed with plastic bending/polygonization. More specifically, it has also been consistently observed that the particular <112> direction then becomes the tilt axis of the plastic deformation in the respective grain. This suggests a correlation of the proximity of certain <112> line directions to the direction of electron flow with the occurrence of plastic behavior.

We now recap our main observations up to this point. Almost immediately upon the application of high-density current flow, Cu grains behave plastically (crystal bending, polygonization, or simply rotation). We confirm that when large single grains spanning across the cross-section of the Cu lines are exhibiting crystal bending (and/or crystal polygonization), the rotation axis of this plastic deformation, which is always one of the <112> of the 12 possible slip systems in FCC crystals, was found to be very close (within 10°) to the direction of the electron flow, as illustrated in Fig. 6.17a. This particular <112> is also always the closest <112> to the direction of electron flow. This finding thus suggests that the proximity of a <112> direction in the grain to the direction of the length of the line is correlated to the occurrence of plastic behavior in a given grain.

This particular finding might have an important practical implication. If all the grains exhibiting crystal bending/polygonization are those with a <112> direction that falls closely within the direction of the electron flow, then we could propose that if a grain is oriented such that none of its <112> direction falls within 10° of the electron flow direction, then this grain would be less susceptible to plastic deformation induced by electromigration. Such grains have their crystallographic orientations in the direction of the electron flow if the lines fall within the shaded regions as shown in Fig. 6.17b. Therefore, it could be proposed that these are the particular in-plane textures of Cu interconnect lines that might give the wires lower susceptibility towards electromigration-induced plastic deformation, or in other words, higher resistance to electromigration later damage.

## 6.3 Plasticity and materials degradation mechanisms in copper interconnects

Most interconnect metals are aggregates of crystalline grains. The crystalline lattice of each grain has a characteristic orientation, and a polycrystal is thus characterized by a distribution of orientations: its texture. Texture governs many of the physical, electrical and mechanical properties of poly-

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crystalline materials. In metallic conductor lines in microelectronics integrated circuits, texture has been known to play important roles in the performance and reliability of the conductors, for instance in electromigration (Vanasupa *et al*., 1999).

Plastic deformation was observed in damascene Cu interconnect test structures during an *in situ* electromigration experiment and before the onset of visible microstructural damage (i.e. voiding) using a synchrotron technique of white-beam X-ray microdiffraction. In this section, the extent of this electromigration-induced plasticity is shown to be dependent on the texture of the Cu grains in the line (Budiman *et al*., 2007a; 2007b; 2009). Furthermore, this dependence on texture has fundamental implications in terms of materials degradation mechanisms in Cu interconnects. We propose that this effect manifests itself in the increased effective diffusivity in the Cu interconnects during electromigration which expedites the degradation mechanisms leading to the eventual catastrophic events of failures (Budiman *et al*., 2007a; 2007b; 2009).

### 6.3.1 Electromigration-induced microstructural changes in Cu interconnects: effects of texture

In this section, we discuss a different set of Cu lines fabricated by a different manufacturer. This set of Cu lines differs with the previous set in a few ways; chief among them is texture. Again using the synchrotron technique of white-beam X-ray microdiffraction, we follow the evolution of plasticity in Cu polycrystals during similar electromigration experiments as in the previous section. We find strong texture dependence and propose a model to explain such prominent observation. In this set of samples, the Cu lines were surrounded by two different sets of dielectric materials. This has enabled us to also study the effect of dielectric constraints.

*Experimental*

The interconnect test structure used here (shown in Fig. 6.18) is a variation of a back-end-of-line (BEoL) process for a 65 nm CMOS technology manufactured by AMD, Inc. (Budiman *et al*., 2007a; 2007b; 2009). In this technology, the dual-damascene Cu fill process includes a standard Ta-based barrier and Cu seed, electroplated Cu fill, post-plating anneal, chemical-mechanical polish and a dielectric cap layer. Two different inter-layer dielectrics (ILD) were integrated with copper: Cu/low-*k* ILD (low-*k* = chemical vapor deposition (CVD) carbon-doped oxide) and Cu/hybrid ILD (hybrid = Cu/low-*k* at the line level and Cu/fluorine-doped tetraethyl orthosilicate (FTEOS) at the via layer). Both ILD materials were studied in order to provide a comparison of the extent of plasticity. The metal two (M2) lines were studied

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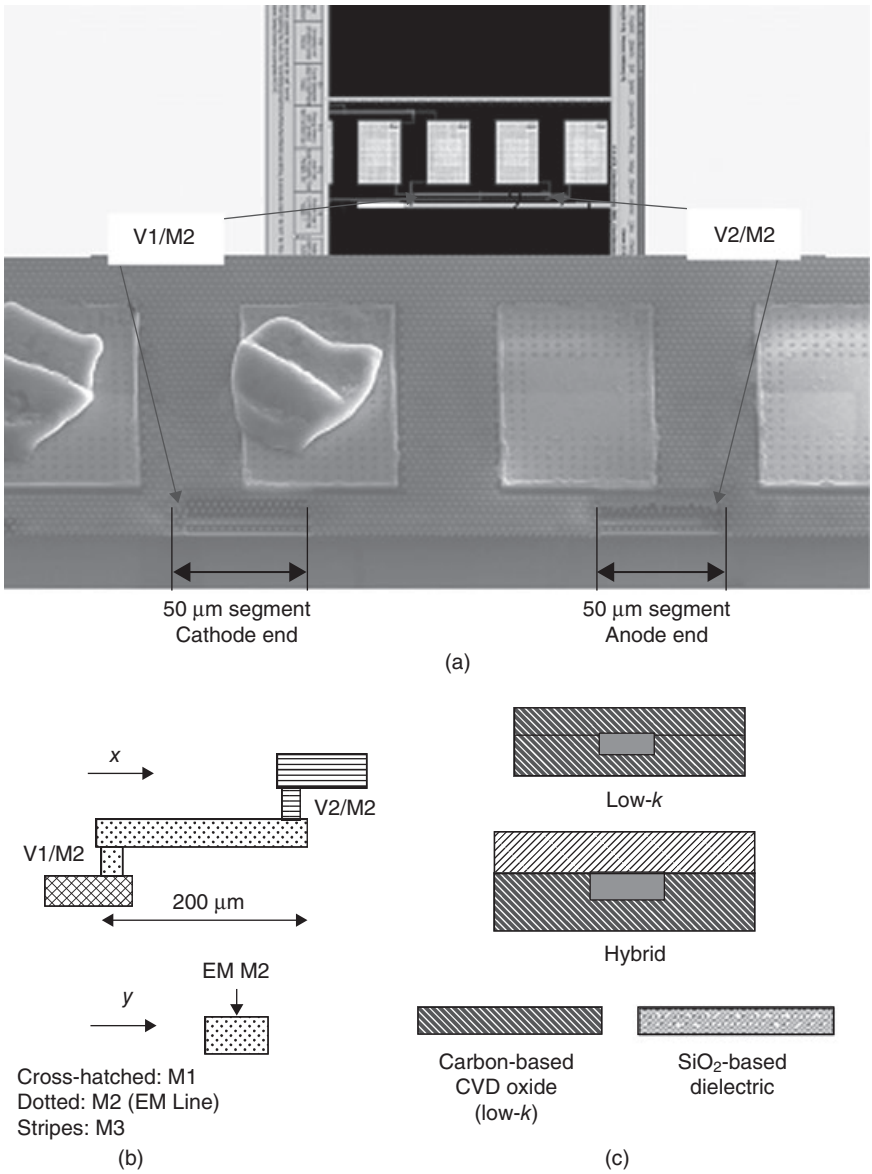


*6.18* SEM images and schematic drawings of the Cu interconnect test structures in this experiment (Budiman *et al.*, 2007a; 2007b; 2009): (a) SEM image of the test structure; (b) *in situ* EM experiment; (c) two sets of test structures of different dielectric schemes: low-*k* versus hybrid.

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after partial removal of the top dielectric to expose the capped Cu lines (Fig. 6.18a). In these electromigration tests, the current was forced from the wide, upper metal layer (M3) into narrow M2 (called a V2M2 test) or from a wide lower metal layer (M1) into a narrow M2 (referred to as a V1M2 test). Both structures are designed to force failure in M2 at its critical dimension.

The first set of test structures consists of 200 μm-long lines, approximately 0.2 μm thick, and 0.5 μm wide. Owing to limited beam time, typical of synchrotron experiments, only segments of 50 μm length at both cathode and anode ends of the line were studied (Fig. 6.18a). The dielectric is carbon-based CVD oxide ('low-*k*' in Fig. 6.18c). The second set of interconnect test structures was prepared with dimensions similar to those of the first one, but with the hybrid ILD material ($SiO_2$-based). The line length is 200 μm, the thickness is approximately 0.25 μm and the width is 0.7 μm. Similarly, only segments of 50 μm length at both cathode and anode ends of the line were studied.

The experiment was performed on the Beamline 7.3.3 (now Beamline 12.3.2) at the Advanced Light Source, Berkeley, CA. The electromigration test was conducted at 300 °C on a via-terminated test structure (Figure 6.18(b)). The current was ramped up to 2 mA ($j = 2$ MA cm$^{-2}$) and then set at that value for the rest of the test (up to 36 h). The ambient temperature in the synchrotron end-station (hutch) where the tests were performed is 20 °C.

*Electromigration-induced plasticity in copper interconnects*

The *in situ* electromigration observations are described first. Figure 6.19 shows the typical evolution of the Laue diffraction spots during the *in situ* electromigration test. Figure 6.19 is early in the electromigration test (after 36 h of testing). The observed broadening of the Laue diffraction spots (streaking) represents plastic deformation of the Cu grains induced by electromigration (Budiman *et al.*, 2004; 2006a; 2006b; Valek *et al.*, 2002; 2003).

As the electromigration test progresses, plasticity is observed in the Cu grains throughout the line, such as demonstrated in Fig. 6.20a. Plasticity here may manifest itself either in the form of diffraction spot broadening (streaking) or in the form of diffraction spot splitting (into two or even more different spots). The broadening of the diffraction spots represents crystal bending of the Cu grains in the line, whereas the split diffraction spots indicate the formation of low-angle boundaries or sub-grain structures (Budiman *et al.*, 2004; 2006a; 2006b; Valek *et al.*, 2002; 2003).

Not only was plasticity observed, but also the direction of the plastic deformation is generally consistent across grains throughout the segments

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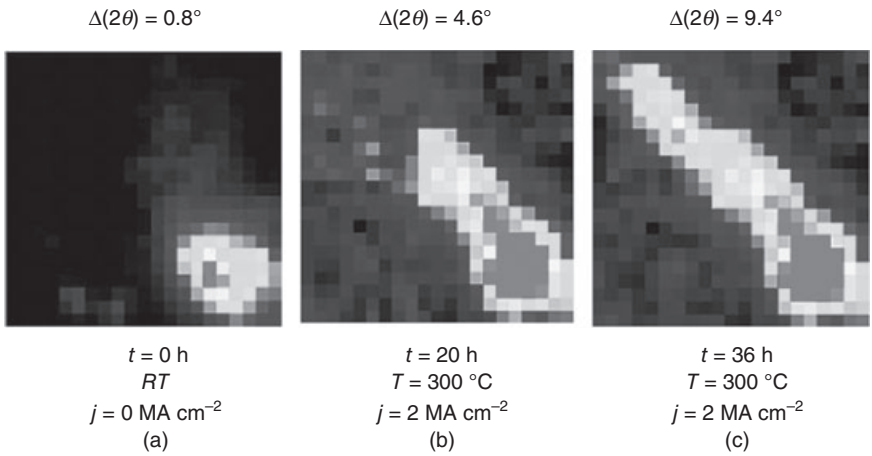


*6.19* The typical evolution of Laue diffractions spots from Cu interconnect test structures during *in situ* electromigration experiments (Budiman *et al.*, 2007a; 2007b; 2009).

of the line under observation, as shown in Fig. 6.20a. This is consistent with our observation on the previous set of Cu lines (Budiman *et al.*, 2004; 2006a; 2006b). Cu grains plastically deform in a direction transverse to the electron flow direction in the line. Such directionality can simply be accommodated by a distribution of same-sign edge dislocations with cores as illustrated in Fig. 6.20b, i.e. with the <112> line direction of the dislocations all lining up along the direction of electron flow in the line.

Exact grain orientation mapping of these Cu lines unfortunately could not be obtained in the present study. The X-ray spot size (0.5 μm × 0.5 μm) used in the Beamline 7.3.3 (now Beamline 12.3.2) was relatively large for the dimensions of these state-of-the-art interconnect lines. That makes diffraction spot indexing very difficult and thus mapping of grain orientations and other further quantitative analyses unreliable. The few Cu grains that we show in Fig. 6.20 were among the limited number of grains in the two Cu lines for which indexing of the diffraction spots happens to be sufficiently clear and unambiguous for this analysis. In general, the larger the Cu grains and the more bamboo-like they are, the more they diffract sharply and give numerous diffraction spots, thus giving higher confidence on the reliability of these results. That being said, it is fortunate that the evolution of Cu diffraction spots before and after some period of electromigration testing can still be compared qualitatively, as demonstrated in Fig. 6.19.

The extent of the electromigration-induced plasticity observed in the present samples is now determined. Figures 6.21a and 6.21b show still different additional diffraction spots observed during this experiment (after EM testing of 36 h, at 300 °C and 2 MA $cm^{-2}$ current loading) from Cu lines

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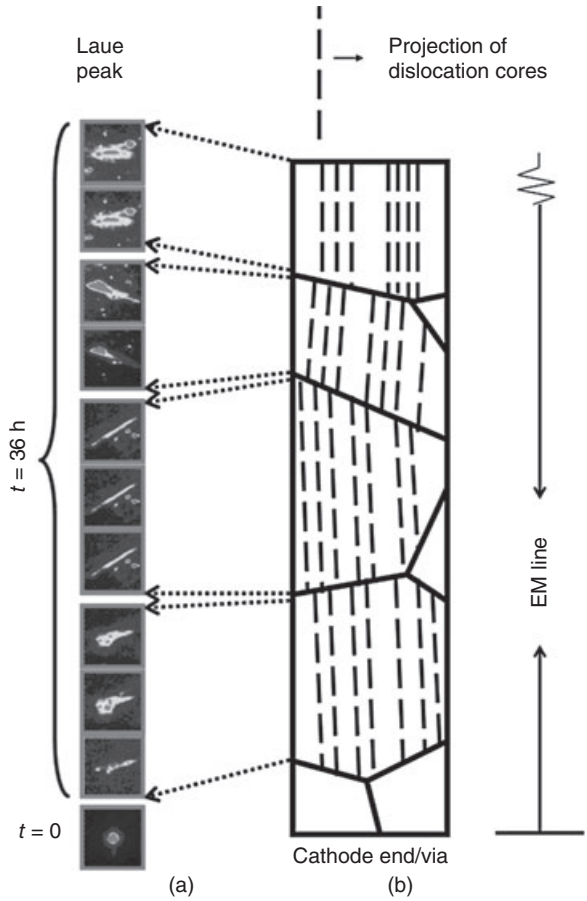


*6.20* Laue diffraction images of the cathode end of the line after 36 h of testing (Budiman *et al.*, 2007a; 2007b; 2009): (a) streaking and/or splitting of Cu Laue diffractions spots (each image represents a 0.5 μm step size) throughout a segment of the line observed; (b) Dislocations observed with cores aligned with the direction of the electron flow in the line (consistent with earlier observations in Budiman *et al.*, 2004; 2006a; 2006b) across grains throughout the length of the segment of the line (the grain map is estimated based on the streaking observation; the total line length studied in each cathode or anode end is 50 μm, and the width is 0.5 μm).

with the low-$k$ and the hybrid dielectrics, respectively. The diffraction spots have been converted to $\chi$-$\theta$ angular space, with $\chi$ running along the direction of the length of the line, and $\theta$ across the direction of the width of the line. The $\chi$-$\theta$ angles refer to the plane normals responsible for the Laue streaks.

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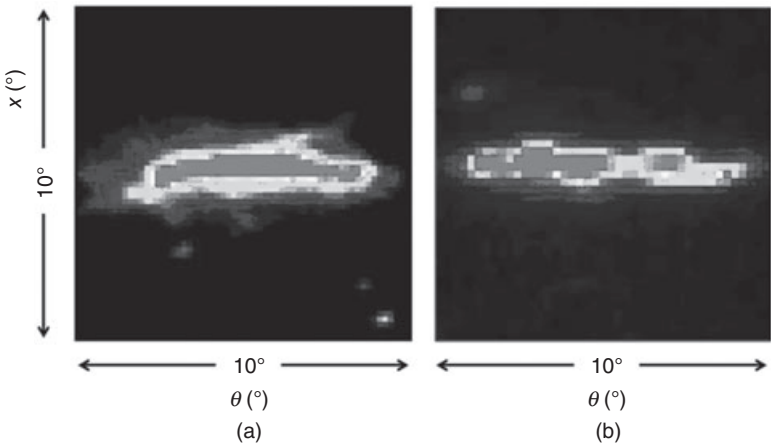


*6.21* A $\chi$–$\theta$ space/contour intensity plot of dielectric effects: the Laue peak streaking/splitting observed from Cu interconnect test structures (Budiman *et al.*, 2007a; 2007b; 2009) with (a) low-*k*, and (b) hybrid dielectrics.

The observed broadening and spot splitting can be used to obtain information about the dislocation structure induced into the grain by electromigration. For instance, from the streak length of Fig. 6.21a, as measured in the digital camera image, and knowing the sample-to-detector distance, we determine the curvature angle of the grain to be 9.8°. Assuming a near bamboo structure, the grain width is the same as the width of the line (0.5 μm), from which we determine the radius of curvature of the grain, $R$ = 2.34 μm. The GND density needed to account for the observed curvature can be calculated from the Cahn-Nye relationship (Cahn, 1949; Nye, 1953), $\rho = 1/Rb$, where $b$ is the Burgers vector. The GND density is then $\rho = 1.68 \times 10^{15}$ m$^{-2}$. The total number of dislocations in the area of the cross-section of the Cu line/grain is approximately 142.

To obtain quantitative information on polygonization walls (subgrain boundaries) from the spot split in Fig. 6.21b, we observe that the Laue spot splitting, $\Delta_\theta = 9.1°$. From this misorientation and Burgers' model of a small-angle grain boundary, $\Delta_\theta = b/L$, where $L$ = dislocation spacing, we find that $L$ = 16 Å which amounts to a total of 110 dislocations in the subgrain boundaries in the cross-section of the Cu line/grain. This translates to a GND density of $\rho = 1.12 \times 10^{15}$ m$^{-2}$.

The extent of the plasticity as described here ($\rho \sim 10^{15}$ m$^{-2}$) is observed across all grains throughout the segments of both lines with different dielectric schemes. The significance of the difference in our analysis above, in terms of the extent of the plasticity, as well as, its manifestation (grain bending versus polygonization) between the two Cu lines with different

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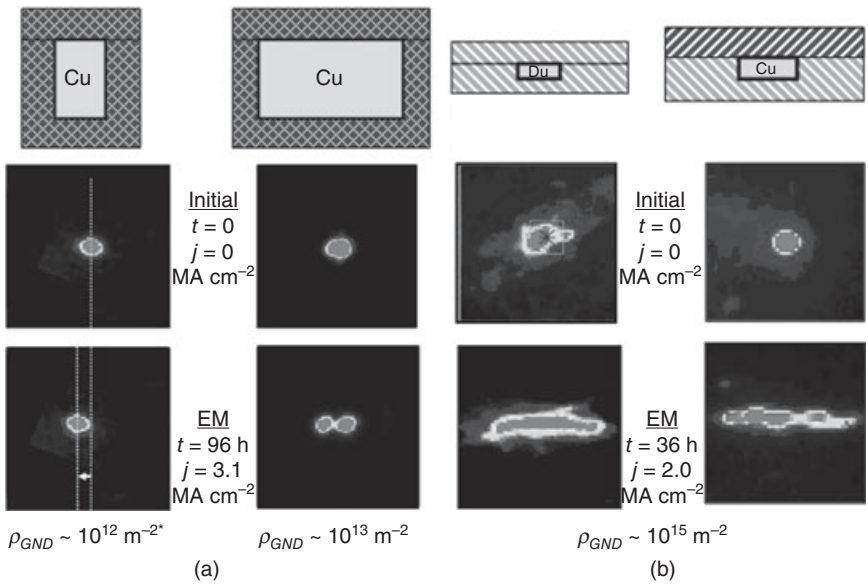
dielectric schemes requires added confirmation. Nevertheless, they provide a general indication of the extent of plasticity in these Cu lines.

*Effects of texture*

Compared with the typical observation of the extent of the electromigration-induced plasticity in the previous set of Cu interconnect lines (Budiman *et al.*, 2004; 2006a; 2006b), this set of samples exhibits at least a two-order of magnitude difference, in terms of GND density (Fig. 6.22). The samples studied in the previous section (referred to as 'Samples A') exhibited $\rho \sim 10^{12}$–$10^{13}$ m$^{-2}$ (Budiman *et al.*, 2004; 2006a; 2006b), and the samples in this section (referred to as 'Samples B') exhibited $\rho \sim 10^{15}$ m$^{-2}$ (Budiman *et al.*, 2007a; 2007b; 2009). Samples A and B differ fairly significantly in dimensions, as well as the dielectric materials used, as shown in Fig. 6.22 (the dimensions are to scale).

Figure 6.22 shows the typical evolution of the Laue reflections from the Cu lines from the initial state (room temperature, $j = 0$, $t$ = time = 0) to the electromigration state (after some electromigration, $T = 300\,^{\circ}$C, $j \sim$




*6.22* Schematics of the cross-sections, typical evolution of Cu Laue diffraction spots (from 'Initial' to 'EM' states), and the typical densities of GNDs implied by the extent of streaking/splitting of Laue peaks: (a) samples A (Cu lines reported in Budiman *et al.*, 2004; 2006a; 2006b); and (b) samples B (Cu lines reported in (Budiman *et al.*, 2007a; 2007b; 2009). (*taken as that of typical annealed metals).

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2.0–3.1 MA $cm^{-2}$, $t$ ~ 36–96 h). Care was taken in order for the observed intensity contours in the $\chi$-$2\theta$ co-ordinate in Fig. 6.22 to be similar (the windows all cover areas of squares of a range of 7° to 10° in angle space, and the threshold of the lower-bound intensity display was set to be similar). Thus, it is obvious from the relative apparent difference in the extent of streaking/splitting of the Laue diffraction spots that the level of plastic deformation that developed during the course of electromigration in Samples B is distinctly larger than that of Samples A.

As the two sets of samples (Samples A and B) under investigation are provided by different integrated circuit manufacturers, it is not possible to completely quantify the process differences (dielectric type, materials processing and thermal history) in their technologies in this section. It is known that the two sets of samples differ in terms of dimension and dielectric materials used; however, it is assumed that the main difference, as far as electromigration-induced plasticity is concerned, is the crystallographic texture of the Cu lines. From the texture analysis conducted in our previous study (Budiman *et al*., 2004), we know that Samples A have a rather weak (111) texture. As mentioned earlier, the exact grain mapping for the present study (Samples B) could not be obtained; however, Samples B came from the same manufacturer of the inlaid Cu lines studied by Besser *et al*. (2001). It is therefore reasonable to assert that Samples B would have the typical strong (111) texture as observed by Besser *et al*. (2001).

Although other process differences between these two sets of samples, including dimensions and dielectric materials, are acknowledged, we believe that these differences cannot satisfactorily explain the differences in the extent of plastic deformation. For example, the Cu in Samples A is surrounded completely by dielectric material, which is a fluorinated $SiO_2$-based dielectric and, thus, generally believed to constrain the Cu lines better, and this should result in less plastic deformation. This is consistent with our observation of Samples A compared with Samples B, but the different dielectric schemes in Samples B, do not appear to affect the level of plasticity in the Cu lines. Another example involves the size effect. Wider lines seem to exhibit more plastic deformation in our previous study (Budiman *et al*., 2004; 2006a; 2006b), such as also shown in the previous section. However, Samples B are much narrower, and also much smaller in all cross-sectional dimensions, than Samples A, but Samples B exhibits two orders of magnitude more electromigration-induced plasticity.

Figure 6.23 is a summary of the known information about the Cu lines in Samples A compared with Samples B. First, Samples A shows a weak (111) texture, and we found the extent of electromigration-induced plasticity of the order of $\rho \sim 10^{12}$–$10^{13}$ $m^{-2}$. Subsequently, Samples B was found with $\rho \sim 10^{15}$ $m^{-2}$ after similar electromigration conditions, a significantly larger amount of electromigration-induced plasticity. Besser *et al*. (2001)

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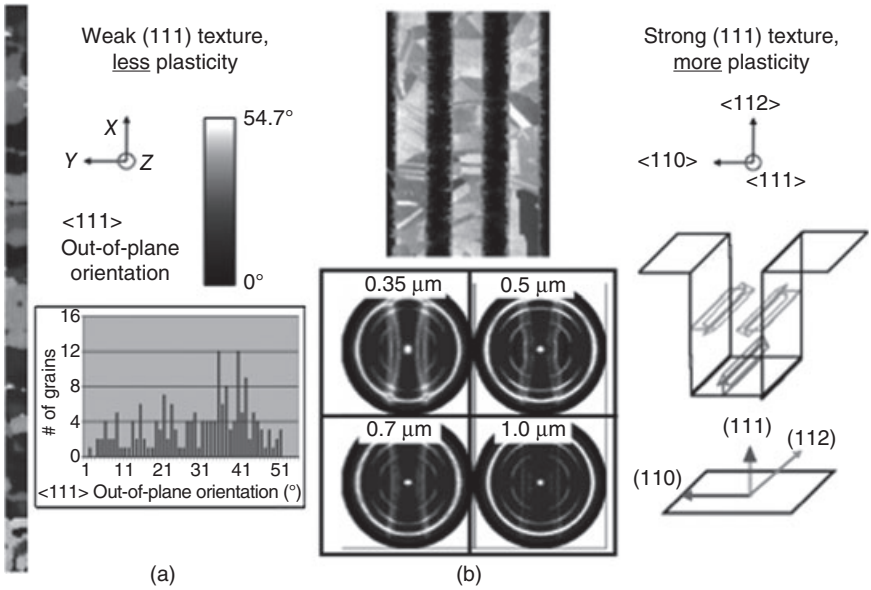


*6.23* Comparison the texture correlation of: (a) samples A, Cu lines reported in Budiman *et al.* (2004; 2006a; 2006b), which have a weak (111) texture, and 'less plasticity,' and (b) samples B, Cu lines reported in Budiman *et al.* (2007a; 2007b; 2009), which have strong (111) texture, and 'more plasticity.' The schematic on the right illustrates that the strong preferred in-plane orientation of (111) grains leads to a preferred <110> to the sidewalls and <112> along the direction of length of the lines (courtesy of Besser *et al.*, 2001).

suggested that Samples B have the typical strong (111) texture. This observation of significantly larger electromigration-induced plasticity in Samples B than in Samples A, is consistent with our earlier observation, as described in the previous section, that the occurrence of plastic deformation in a given grain can be strongly correlated with the availability of a <112> direction of the crystal in the proximity of the direction of the electron flow in the line (within an angle of 10°). In <111> out-of-plane oriented grains in a damascene interconnect scheme, the crystal plane facing the sidewall tends to be a {110} plane, so as to minimize the interfacial energy (Paik *et al.*, 2004; Besser *et al.*, 2001; Sanchez and Besser, 1998). Therefore, it is deterministic rather than probabilistic that the (111) grains have a <112> direction nearly parallel to the direction of electron flow or the direction of the length of the line. This is illustrated in Fig. 6.23b.

In Samples B, most grains are <111> in out-of-plane orientation (such as shown in the focused ion beam mapping in Fig. 6.23b), and thus prefer energetically to have the <110> directions normal to the sidewalls, thus causing a <112> direction to be very close to the direction of the electron

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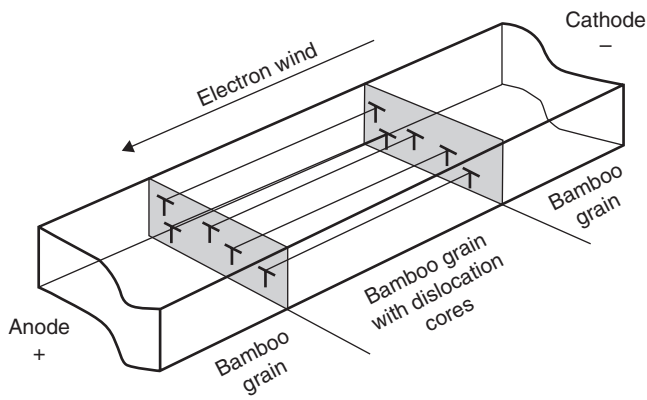
flow. When this condition is met, our proposed correlation discussed in the previous section (Budiman *et al.*, 2004; 2006a; 2006b) suggests that plasticity occurs in these Cu grains upon electromigration, and not only did it occur in this study, the extent of the plasticity here was rather extreme. Samples A, in the meantime, have only a few grains that are <111> in out-of-plane orientation, which leads to the occurrence of plasticity only in these few grains in the Cu lines after electromigration. In most other grains (i.e. non <111>-oriented grains), a <112> direction of the Cu crystal is not likely to be the direction of the electron flow of the lines. Thus, plasticity was not observed in many grains in the Cu lines of Samples A.

## 6.3.2 Plasticity-amplified diffusion in electromigration

The observed plasticity described above (Fig. 6.20) leads to a concentration of same-sign edge dislocations with cores running along the direction of electron flow, as illustrated three-dimensionally in Fig. 6.24. When this configuration of same-sign edge dislocations extends through grains along the full length of the interconnect lines, the dislocation cores can serve as additional paths for diffusion of atoms from one end of the interconnect line to the other. Dislocation cores are, in general, already recognized as fast diffusion paths (Baker *et al.*, 2000), but in this configuration especially, their contribution to the overall migration of atoms from the cathode to the anode end of the line is even more pronounced. Furthermore, when the concentration of these dislocations becomes high enough, their contribution to the overall effective diffusivity ($D_{\text{eff}}$) can no longer be neglected.

In this context, the effective diffusivity can be written as:




*6.24* Schematic of a grain containing same-sign edge dislocations with cores running along the direction of the electron flow in the interconnect line.

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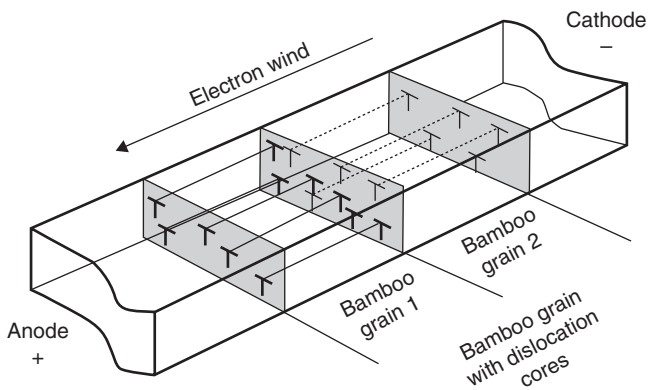
$$D_{\text{eff}} = \frac{\delta}{h} D_{\text{int}} + \rho a_{\text{core}} D_{\text{core}}^{\text{eff}} \quad [6.2]$$

where $a_{\text{core}}$ is the cross-sectional area of dislocation cores, $D_{\text{core}}^{\text{eff}}$ is the effective core diffusivity, $\rho$ is the dislocation density, and $\delta$, $h$ and $D_{\text{int}}$ are the effective interface diffusion thickness, the height of the line and the diffusivity of the interface, respectively. It is necessary here to use $D_{\text{core}}^{\text{eff}}$, the effective core diffusivity (instead of simply $D_{\text{core}}$, the core diffusivity), because for the dislocation cores to have an effect on mass flow along the full length of the line, a continuous diffusion path (across grains) must be available for atoms to transport from the cathode end to the anode end of the lines. Considering the mostly bamboo grain structure that our interconnect lines have (as shown in Fig. 6.20), this requires consideration of grain boundary diffusion, as atoms eventually hit the grain boundaries and have to travel some distance in the grain boundary before finding another set of dislocation cores (belonging to the neighboring grain) to continue their travel to the other end of the line. This is illustrated schematically in Fig. 6.25. Thus, the effective core diffusivity, $D_{\text{core}}^{\text{eff}}$, here is defined as the effective diffusivity along the dislocation cores when the effect of the grain boundary diffusion is taken into account.

It is obvious that only when the effect of the grain boundary diffusion is negligible (or in other words, the grain boundary diffusion is a fast enough process), can dislocation cores provide a competitive alternative diffusion path and influence the overall effective diffusivity $D_{\text{eff}}$ as suggested in




*6.25* Illustration of bamboo grains with dislocation cores running along the direction of the electron flow in the line under electromigration bias. Dislocation cores from one grain end at the grain boundaries. Atoms traveling across multiple grains must diffuse along grain boundary regions, before finding another set of dislocation cores in the next grain.

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equation 6.2. In order to study quantitatively the impact of this grain boundary diffusion on the overall dislocation core diffusion ($D_{\text{core}}^{\text{eff}}$), we derive the kinetics for such a model and arrive at the expression below for $D_{\text{core}}^{\text{eff}}$ (the full derivation is provided in Budiman *et al.*, 2009),

$$D_{\text{core}}^{\text{eff}} = D_{\text{core}}\left[\frac{2\delta_{\text{gb}}D_{\text{gb}}L}{2\delta_{\text{gb}}D_{\text{gb}}L + r_{\text{core}}^2 D_{\text{core}}\ln(R/r_{\text{core}})}\right] \quad [6.3]$$

where $\delta_{\text{gb}}$ and $D_{\text{gb}}$ are the effective width and diffusivity of the grain boundary, respectively, $L$ *is the* overall length of the diffusion path, $r_{\text{core}}$ is the radius of the dislocation core, and $R$ is the mean distance in the grain boundary to the next dislocation core.

The influence of grain boundary diffusion on the overall/effective dislocation core diffusivity $D_{\text{core}}^{\text{eff}}$, thus depends on the relative magnitude of the two terms in the denominator in the equation [6.3]. If:

$$2\delta_{\text{gb}}D_{\text{gb}}L >> r_{\text{core}}^2 D_{\text{core}}\ln(R/r_{\text{core}}) \quad [6.4]$$

then, as evident from equation [6.3], $D_{\text{core}}^{\text{eff}}$ degenerates into simply $D_{\text{core}}$ or, in other words, there is very little influence of the grain boundary diffusion in the overall scheme in Fig. 6.25. If the reverse is true, $D_{\text{core}}^{\text{eff}}$ is much smaller than $D_{\text{core}}$, and the grain boundary slows down the overall diffusion significantly.

Referring now to the textbook values for grain boundary and core diffusion compiled in Table 6.1 (Cai *et al.*, 1999; Dickenscheid *et al.*, 1991; Frost and Ashby, 1982; Gan *et al.*, 2006), and shown in Table 6.2, it is evident that

*Table 6.1* Values used to determine the influence of grain boundary diffusion on the overall transport kinetics in the Cu line under EM. The diffusivities ($D_{\text{gb}}$, $D_{\text{core}}$) are described in the usual way by $D = D_{\text{o}}\exp(-E_{\text{A}}/kT)$ where $E_{\text{A}}$ is the activation energy, $D_{\text{o}}$ is the pre-exponential constant, and $k$ is the Boltzmann's constant. The subscripts *gb* refers to grain boundary diffusion

| Variable | Value | Reference/remarks |
|---|---|---|
| $T$ | 300 °C = 573 K | Following $T_{\text{test}}$ in 6.3.2 'Experimental' |
| $E_{\text{A,gb}}$ | 1.08 eV | Frost and Ashby, 1982; Gan *et al.*, 2006; Cai *et al.*, 1999; Dickenscheid *et al.*, 1991 |
| $\delta_{\text{gb}}D_{\text{gb}}$ | $1.6 \times 10^{-24}$ m$^3$ s$^{-1}$ | Calculated (Frost and Ashby, 1982) |
| $L$ | 1 μm | Estimated (Budiman *et al.*, 2009) |
| $r_{\text{core}}$ | 0.25 Å | Frost and Ashby, 1982 |
| $E_{\text{A,core}}$ | 1.21 eV | Frost and Ashby, 1982 |
| $r_{\text{core}}^2 D_{\text{core}}$ | $7.3 \times 10^{-36}$ m$^4$ s$^{-1}$ | Calculated (Frost and Ashby, 1982) |
| $\rho_{\text{GND}}$ | $10^{15}$ m$^{-2}$ | As observed in Budiman *et al.*, 2009 |
| $R$ | 22 nm | $R = 1/2\rho_{\text{core}}$ |

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*Table 6.2* Values of the two parameters/terms in equation [6.4] (or denominator of equation [6.3]) calculated from values listed in Table 6.1

| Parameter/term | Value |
|---|---|
| $2\delta_{gb}D_{gb}L$ | $3.2 \times 10^{-30}$ m$^4$ s$^{-1}$ |
| $r_{core}^2 D_{core} \ln(R/r_{core})$ | $5.0 \times 10^{-35}$ m$^4$ s$^{-1}$ |

the $2\delta_{gb}D_{gb}L$ term in equation [6.3], as well as in equation [6.4], is at least four orders of magnitude larger than the $r_{core}^2 D_{core} \ln(R/r_{core})$ term. This leads to the degeneration of $D_{core}^{eff}$ into simply $D_{core}$ in equation [6.3], reducing to equation [6.5]:

$$D_{core}^{eff} \approx D_{core} \quad [6.5]$$

The practical implication of equation [6.5] is that a practically continuous pipe (dislocation core) diffusion path across multiple grains between the cathode end and the anode end of the line is indeed available for atomic transport in the Cu test structures under accelerated electromigration testing.

An 'extreme' assumption would be to take the activation energy for grain boundary diffusion $E_{A,gb}$ to be the $E_A$ for lattice diffusion, which is 2.04 eV (Frost and Ashby, 1982). This is a much higher activation energy than that of grain boundary diffusion. In this case, we show that the combined diffusivity would be dominated by such slow diffusion in the hypothetical 'grain boundary.' The effective transport through dislocation cores in this case would be slowed down by nearly four orders of magnitude owing to the effect of the hypothetical grain boundary. This is shown in Fig. 6.26, which compares calculated diffusivities as a function of temperature for three different schemes of diffusion ($D_{core}$, $D_{core}^{eff}$ 'as it is,' and $D_{core}^{eff}$ 'extreme,' as defined above). The $D_{core}^{eff}$ 'extreme' line is close to four orders magnitude lower than $D_{core}^{eff}$ line (with crosses), which is practically on top of each other with the $D_{core}$ line (with buttons) as suggested by equation [6.5].

It is therefore reasonable to propose that a fully continuous network of dislocation cores running along the direction of the length of the line, slowed only by less than 0.01% by grain boundary diffusion, exists in the Cu interconnect lines studied during electromigration under accelerated test conditions in this study. This makes it a viable alternative for global transport of atoms in Cu interconnects under electromigration bias.

The existence of a viable path of dislocation core diffusion alone, however, is not sufficient to influence the overall kinetics in equation [6.2], that is, if the dislocation density ($\rho$ or $\rho_{GND}$) is not high enough. We discuss this situation below and show the importance of the experimental results described

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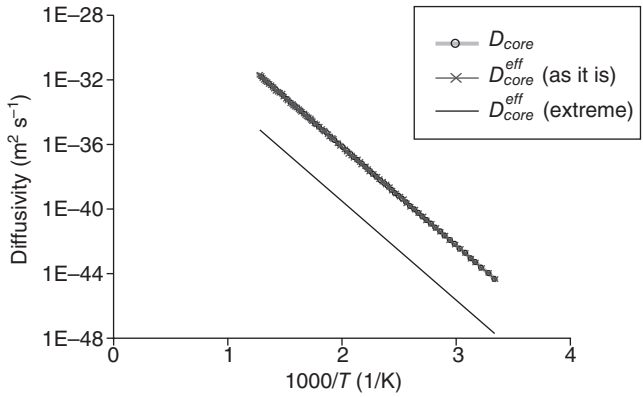


*6.26* Comparison of diffusivities as a function of temperature between $D_{core}$ (only dislocation core diffusion, no grain boundary), $D_{core}^{eff}$ (considering the effect of grain boundary; as it is – as shown in Table 6.2), and an extreme $D_{core}^{eff}$ (considering the effect of grain boundary diffusion as if it is lattice diffusion). Diffusivities were calculated using values summarized in Table 6.1.

in this section in understanding the overall kinetics in Cu interconnect lines under electromigration.

Diffusion along dislocation cores ('pipe diffusion') has been commonly included in models of diffusion-controlled deformation in bulk materials (Frost and Ashby, 1982). Suo (1994) considered the motion and multiplication of dislocations under the influence of an electric current in a conductor line, and suggested that electromigration-driven dislocation multiplication could itself lead to dislocation densities high enough to affect electromigration degradation processes. Oates (1996), however, did not see any diffusivity effects that could be attributed to dislocations in his experimental study. Baker *et al.* (2000) through their experimental study of nanoindented Al lines (width = 1 μm, mean grain size = 1.1 μm) showed that the effect of a dislocation density of $10^{16}$ $m^{-2}$ is similar to diffusion through a grain boundary. These studies all essentially suggest that if the dislocation density is sufficiently high, it may affect the overall electromigration degradation processes in metallic interconnects, and thus could have fundamental implications.

### *Materials degradation mechanisms*

We have, earlier in the manuscript, established that dislocations with cores running along the electron flow direction and densities in the order of $10^{15}$ $m^{-2}$ are present in the Cu lines undergoing electromigration (acceler-

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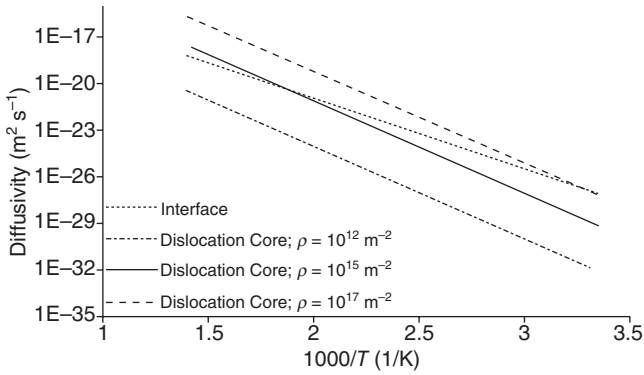


*6.27* Calculated diffusivities as a function of temperature between the interface diffusion path and those of dislocation cores of various densities in Cu interconnect lines ($10^{12}$ m$^{-2}$, $10^{15}$ m$^{-2}$, $10^{17}$ m$^{-2}$). Each diffusion mechanism is assumed to act alone (Budiman *et al.*, 2009).

*Table 6.3* Values used to determine diffusions in Cu interconnects as a function of temperature (Fig. 6.27). $D_o$ is the pre-exponential constant and $E_A$ is the activation energy. The subscripts *int* and *core* refer to interface and core diffusions, respectively. The $\delta$ is the effective interface diffusion thickness, $h$ is the thickness of the Cu lines, and $a_{core}$ is the area of a dislocation core

| Variable | Value | Reference/remarks |
|---|---|---|
| $\delta D_{o,int}$ | $3.4 \times 10^{-19}$ m$^3$ s$^{-1}$ | Based on SiN/Cu (Gan *et al.*, 2006) |
| $h$ | 0.2 μm | Budiman *et al.*, 2009 |
| $E_{A,int}$ | 0.91 eV | Based on SiN/Cu (Gan *et al.*, 2006) |
| $a_{core}D_{o,core}$ | $1.0 \times 10^{-24}$ m$^4$ s$^{-1}$ | For copper (Frost and Ashby, 1982) |
| $E_{A,core}$ | 1.21 eV | For copper (Frost and Ashby, 1982) |

ated test conditions) for 36 h. Figure 6.27 is a comparison of calculated diffusivities as a function of temperature between the interface diffusion path and those of dislocation cores of various densities in Cu interconnect lines ($10^{12}$ m$^{-2}$, $10^{15}$ m$^{-2}$, and $10^{17}$ m$^{-2}$) when each diffusion mechanism is assumed to act alone. The diffusivities are calculated based on diffusion coefficient values in the literature (Frost and Ashby, 1982; Gan *et al.*, 2006) for Cu interconnect lines (Table 6.3), and for the interconnect dimensions as described earlier in this section.

The dislocation density observed in the present study ($\rho_{GND} = \rho_{core} = 10^{15}$ m$^{-2}$) is illustrated as the solid line in Fig. 6.27, illustrating that dislocation core diffusion is on the same order of magnitude as that of interface

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diffusion (the dotted line) at the test conditions ($T$ = 300 °C or *1000/T* = 1.75/K). Thus, a core dislocation density of $10^{15}$ m$^{-2}$ is the dislocation density threshold necessary for dislocation core diffusion to be on a par with interface diffusion. In other words, at this dislocation density the contribution of dislocation cores to the overall/effective diffusivity in the Cu line during accelerated electromigration is expected to be at least the same order of magnitude as interface diffusion and thus cannot be neglected.

It is to be noted, however, that at temperatures at or below 100 °C, the required dislocation density for cores to have a significant contribution to the diffusion would be on the order of $10^{17}$ m$^{-2}$ (the dashed line in Fig. 6.27). These lower temperatures correlate with the typical use or operational conditions of the interconnects. The typical initial (as fabricated) dislocation density in Cu/metallic lines was taken to be $10^{12}$ m$^{-2}$ (following Baker *et al.*, 2000), and the corresponding diffusivity is shown by the dashed-dotted line in Fig. 6.27.

It is therefore reasonable to propose that the contribution from the dislocation core diffusion (the second term in equation [6.2]) can no longer be neglected in the Cu lines now that we have evidence of the existence of such high density of dislocation cores in the real Cu interconnect structure. It is certainly true in the Cu lines investigated in the present study especially during electromigration at accelerated test conditions. The contribution from dislocation cores would enhance the electromigration diffusion, or in other words, the total electromigration flux ($J_{EM}$), since the total or overall diffusion includes the existing, usually-dominant interface diffusion, plus the observed dislocation core or 'pipe' diffusion. The increase in this core diffusion to the point of significance in the overall electromigration diffusion is related to the kind and the extent of plasticity induced by the electromigration process itself (i.e. through the increase in the core dislocation density from the pre-electromigration density $\rho_{core} = 10^{12}$ m$^{-2}$ to the observed density $\rho_{core} = 10^{15}$ m$^{-2}$).

The result of this study gave a key piece of experimental evidence that opens up the possibility that such a high dislocation density may generally be present in the Cu test structures undergoing electromigration. The circumstances and the important implications of this special configuration of dislocation cores for the electromigration degradation processes warrant discussion, as do the electromigration reliability assessment methodologies. With $\rho_{GND} \sim 10^{15}$ m$^{-2}$ observed in this study, and $D_{core}^{eff}$ that is not much reduced by grain boundary diffusion (as derived above and in Budiman *et al.*, 2009), the second term in equation [6.2] (i.e. the contribution of the dislocation core diffusion) can indeed no longer be neglected. This means it will have important implications to the fundamental understanding of the electromigration degradation processes, as well as to the electromigration reliability assessment methodologies.

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## 6.4 Implications for the reliability of advanced copper interconnect schemes

Electromigration is a major reliability concern in the advanced microelectronics industry. This is because of the aggressive scaling of interconnect dimensions and the recent introduction of new materials and processing schemes leading to even more challenges in guaranteeing interconnect robustness against electromigration failure. Understanding the fundamental relationship between electromigration in interconnect lines and parameters of materials and processing that make up the interconnect structures, is thus very important.

In addition, it is also useful, especially for industry, to accurately assess the lifetime of the device under electromigration conditions. This involves taking data under accelerated conditions (such as high temperatures and current densities) and scaling it back to the device operational conditions. This electromigration lifetime extrapolation is commonly based on the well-established Black's Law (Black, 1967). This methodology for extrapolations determines whether a technology is sufficiently reliable against electromigration failure for a given specification, or whether further optimization in process and/or design is needed.

Black's Law (Black, 1967) expresses the median time to failure (*MTF*), or the 50th percentile fail time of a failure population, as:

$$\mathrm{MTF} = A\left(\frac{1}{j}\right)^{n} \exp\left(\frac{E_{\mathrm{A}}}{kT}\right) \qquad [6.6]$$

where $A$ is an empirically-determined constant, $j$ is the current density, $n$ is the current density exponent, $E_{\mathrm{A}}$ is the activation energy to electromigration failure, $k$ is the Boltzmann's constant and $T$ is the absolute temperature.

The figure of merit for electromigration reliability is the use current density (current density at device operational conditions), which is commonly denoted as $j_{\mathrm{use}}$ or $j_{\mathrm{max}}$, and represents the maximum current density the interconnect system can maintain while still guaranteeing a certain failure rate over a certain amount of operation time at use conditions. Therefore the current density exponent $n$ is crucial, as the extrapolated failure time (i.e. device lifetime at use/operational conditions) is very sensitive to it.

Although Black's equation, equation [6.6] is widely used, the value for the current density exponent and its implications to electromigration lifetime prediction are still much debated (Budiman *et al*., 2010; Hau-Riege, 2004; Hu *et al*., 1999; 2007; Kirchheim and Kaeber, 1991; Roy and Tan, 2008; Shatzkes and Lloyd, 1986). Under the common atomistic description of electrotransport (Verhoeven, 1963), the flux in the electromigration of a

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metallic line is proportional to the current density and the product of flux and time (i.e. MTF) and corresponds to the removal of a certain volume of matter per unit length (i.e. the cross-section area) of the interconnect line, which is a necessary condition for failure. Thus we have MTF ~ $j^{-1}$ (i.e. $n$ = 1). This description is usually associated with a void growth limited failure mode (Hau-Riege, 2004; Hau-Riege *et al*., 2002), as opposed to a void nucleation limited mode, which has also recently been supported by experimental observation (Zschech *et al*., 2004). These concepts appear to be applicable to the case of Cu interconnects (Hau-Riege *et al*., 2002).

However, it has been widely observed that the current density exponent $n$ is usually found in real cases to be >1 (Budiman *et al*., 2010; Hau-Riege, 2004; Hu *et al*., 1999; 2007; Kirchheim and Kaeber, 1991; Roy and Tan, 2008; Schafft *et al*., 1985; Shatzkes and Lloyd, 1986) as opposed to $n$ = 1 for the prevailing model of void growth limited failures. This suggests that there is an extra dependency on $j$, under accelerated test conditions. This extra dependency has been attributed to the effect of Joule heating (Bobbio and Saracco, 1975; Kirchheim and Kaeber, 1991; Schafft *et al*., 1985; Sigsbee, 1973). Joule heating is the process by which the passage of an electric current through a conductor releases heat. It is caused by interactions between electrons that make up the body of the conductor. At higher $j$ (accelerated/test conditions), more electrons are passing in the interconnect line, causing more heating, and thus a higher temperature (making it even higher than the accelerated/test temperature), leading to amplification of electromigration diffusion in the interconnect lines, and thus earlier failure events. This manifests in the Black's Law as an extra dependency on $j$, or in other words, the deviation of $n$ from unity (and/or from $n$ = 2, for that matter).

### 6.4.1 Inflated current density exponent *n*

If $\rho$ increases with $j$, then we find that $D_{\text{eff}}$ (the overall/effective diffusivity of the electromigration process) also increases with $j$. Consequently, there is an extra electromigration flux, and thus an extra reduction in the time to failure of the device with increasing $j$. This is an extra dependency on $j$, which manifests itself in the value of the current density exponent $n$ in Black's equation [6.6], being >1.

Kirchheim and Kaeber (1991) first experimentally observed the MTF dependency on current density $j$ in an Al conductor line, for a wide range of $j$, such as shown in Fig. 6.28 (the solid black dots with error bars were the original data points). It clearly shows that at low current densities, the MTF data is best fit by $n$ = 1 (straight solid line), whereas at higher current densities, the MTF data is better fit by $n$ >1 (curved dotted line). Kirchheim and Kaeber (1991), however, suggested that these deviations occurring at higher current densities might be caused by Joule heating.

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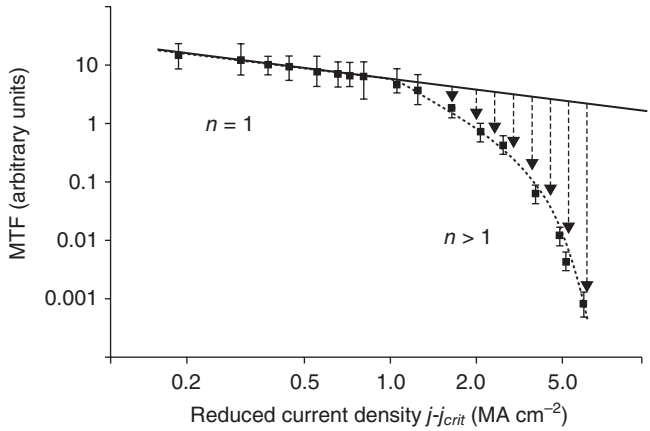


*6.28* Kirchheim and Kaeber's experimental MTF data (reproduced manually here to the highest accuracy possible from Kirchheim and Kaeber (1991); for clarity and improved image resolution) as a function of reduced current density, $j - j_{crit}$ (all the solid features); the dotted and dashed lines have been added as described in the text (courtesy of Kirchheim and Kaeber, 1991).

Similar experimental observation of the MTF dependency on current density $j$ for a wide range of $j$, in the Cu interconnect lines has recently been reported by Budiman *et al.* (2010). Figure 6.29 shows the electromigration failure time as a function of current density in the electromigration tests performed on Cu interconnect samples very similar to the ones studied in the previous section (Budiman *et al.*, 2007a; 2007b; 2009). Both samples were fabricated in the same wafer fabrication facility using the same 65 nm CMOS technology node. Thus, we can reasonably expect similar microstructural evolution during electromigration (as described in the previous section as well as in Budiman *et al.*, 2009) also occurred with this set of samples (Budiman *et al.*, 2010).

The median time to failure (MTF) in Fig. 6.29 is represented by the solid circle, whereas the error bar represents the range of the failure times coming from the 20 samples at each of the test conditions. All failure times are normalized with respect to the minimum MTF observed in the present study. No actual failure times are given here for proprietary reasons. The current densities are also normalized with respect to the minimum value in the present study, which is 0.5 MA cm$^{-2}$. The data can be broadly divided into two groups; the low current densities (with $\ln j / j_{min} < 1.6$, or $j <$ 2.5 MA cm$^{-2}$) and the high current densities with $j > 2.5$ MA cm$^{-2}$. As we can see in Fig. 6.29a, the data in the low $j$ range is best fit by a straight line with a slope of –1.1, which indicates $n = 1.1$ in Black's equation (Black, 1967) whereas in the high $j$ range, $n = 1.7$. These results are consistent with the

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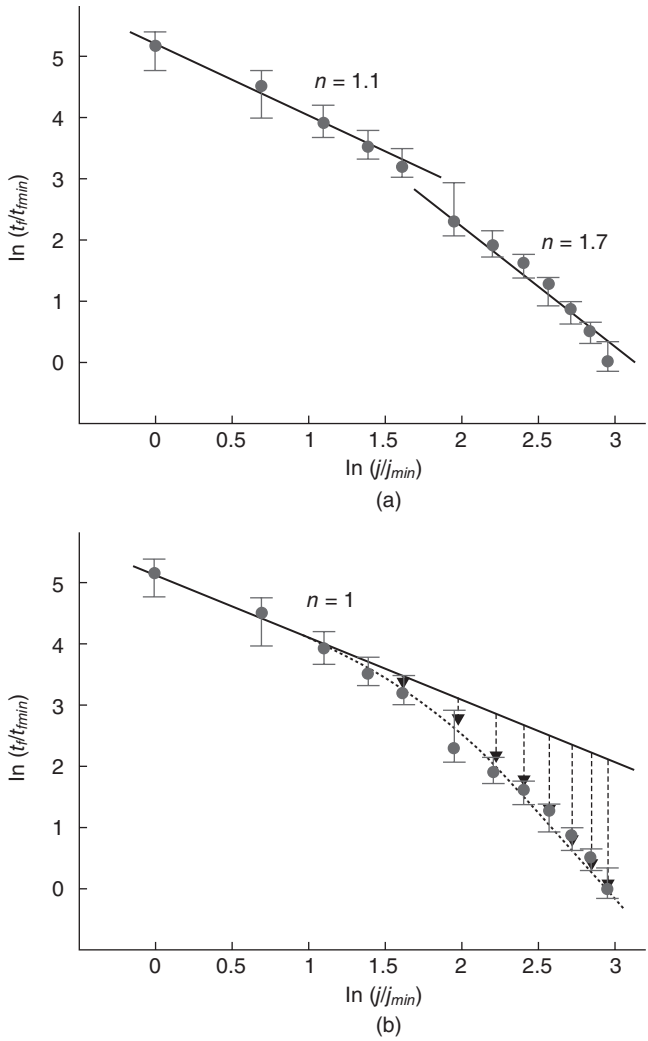


*6.29* Electromigration (EM) test data/results from the Cu interconnect lines (Budiman *et al.*, 2010) showing (a) $n = 1.1$ in the low $j$ range, whereas $n = 1.7$ in the high $j$ range, or, alternatively, (b) that $n$ is principally 1 (the solid line) but MTF tends to be depressed in high $j$ range (the dotted line) owing to extrinsic effects (the dashed line/arrow), as suggested by Kirchheim and Kaeber (1991). Note that the EM failure time data (the median as well as range; the solid circle and the error bar) as a function of $j$ are identical between (a) and (b).

trend in Cu electromigration that has been reported recently by several researchers (Hu *et al.*, 1999; 2007; Roy and Tan, 2008), most notably by Hu *et al.* (2007) who reported $n = 1.1$ and 1.8 for low and high current densities, respectively, under similar electromigration test conditions.

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Alternatively, we may also suggest that $n$ is principally 1 (especially true in the lower $j$ range as indicated by the solid line in Fig. 6.29b), but that the MTF tends to be depressed in the high $j$ range, which, in turn, causes the $n$ value to deviate from the $n = 1$ line. Kirchheim and Kaeber (1991) attributed this extra depression of MTF in the high $j$ range on a Joule heating effect. Earlier *in situ* studies (Budiman *et al*., 2004; 2006a; 2006b, 2007a; 2007b; 2009; Kai *et al*., 2008a; 2008b; Valek *et al*., 2002; 2003) observing microstructural changes and their evolution in Al as well as Cu interconnects during electromigration tests have also suggested EM-induced plasticity that can lead to new paths for electromigration transport which could also be responsible for this deviation (Budiman *et al*., 2009).

Plasticity, especially in the form described in this chapter as well as by Budiman *et al*. (2007a; 2007b; 2009) in Cu interconnects schemes could just as likely be the source of such deviations of MTF dependency on $j$ at high current densities (Budiman *et al*., 2009; 2010). As $j$ increases, plasticity also increases leading to increasingly higher electromigration fluxes (the dashed, arrowed lines in Fig. 6.28 as well as in Fig. 6.29) and, thus, increasingly lower MTF, and therefore eventually a current density exponent $n > 1$ has to be used to fit the failure time distribution.

However, if this deviation were caused by Joule heating alone then the effects would not be permanent; if the same sample were subsequently subjected to electromigration testing with low $j$, the degradation in failure times should not be retained. This hypothesis motivated us to study the second set of samples: the 'pre-damaged' samples (Budiman *et al*., 2010). The pre-damaged samples are the Cu interconnect samples that had been previously subjected to accelerated electromigration testing (at $T = 350$ °C and $j = 3.5$ MA cm$^{-2}$ for a brief period of 50 h), i.e. the 'pre-damaging' phase. If Joule heating is wholly responsible for the deviation from $n = 1$, then the effects of this 'pre-damaging' phase would not be permanent and the failure times for this second set of samples should be about the same as for the nominal samples. On the other hand if the 'pre-damaging' phase causes a permanent change in the diffusional pathways, then the effects *would* be permanent and the degraded failure times would be retained for electromigration testing with low $j$ (or in other words the failure times for the second set of samples should be significantly lower than those of the nominal samples). This is the main focus of the next subsection.

### *Joule heating effect versus electromigration-induced plasticity*

A recent study comparing two sets of samples in which the main difference was the initial microstructures of Cu interconnects (Budiman *et al*., 2010) aims to provide insights into this question. The first set has been described above (Fig. 6.29) and is expected to have typical initial microstructures of

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annealed Cu grains. The second set is expected to have plastically deformed microstructures based on our earlier plasticity observations on similar Cu interconnect samples (Budiman *et al*., 2007a; 2007b; 2009). The experiment has been described in great detail by Budiman *et al*. (2010).

Electromigration test results for the two sets of samples: nominal versus 'pre-damaged' are compared in Fig. 6.30a. The electromigration test results of the nominal samples have been discussed above (Fig. 6.29). The median times to failure (MTFs) here are again represented by the solid features (circles for nominal samples and squares for the 'pre-damaged' ones), and the error bars represent the ranges of the failure times coming from the 20 samples from each group at each of the test conditions. All failure times are again normalized with respect to the minimum MTF observed in the present study. The current densities are also normalized with respect to the minimum value, which is 0.5 MA $cm^{-2}$. It is clear from these data sets that there is a significant difference in time to failure between samples from the two different groups especially in the low $j$ range ($\ln j/j_{min} < 1.95$ or $j <$ 3.5 MA $cm^{-2}$).

In Fig. 6.30b, we consider just the MTFs of two sets of samples (the solid data points; without the error bars for clarity). The significant difference in the MTFs between the two sets of samples in the low $j$ range suggests that Joule heating alone cannot be responsible for the deviation of MTF from the $n = 1$ line at the high $j$ range such as shown in Fig. 6.29b. However, because the 'pre-damaging' phase was done at accelerated conditions of high temperature and high current density (at $T = 350\,°C$ and $j = 3.5$ MA $cm^{-2}$) even though for a very brief period of time (50 h), it could perhaps cause very aggressive void growth such that the failure times for the second set of samples become somewhat lower than those of the nominal samples. In order to account for this equivalent lifetime used by the 'pre-damaging' phase, we now add the 'hypothetical' data points (i.e. the 'plus' and 'minus' signs) to indicate the shortened lifetime of the 'pre-damaged' samples if the 'pre-damaging' phase degrades the MTF more than its nominal 50 h owing to the very aggressive void growth.

The 'equivalent' lifetimes used by the 'pre-damaging' phase (the 'plus' and 'minus' signs) here were calculated using the proportionality assumption (i.e. $MTF(j)^n$ = constant; $MTF' = (j/j')^n MTF$; for the 'plus' signs, as the 'pre-damaging' phase was actually done at $j$ = 3.5 MA $cm^{-2}$ for 50 h, the 'equivalent' lifetime used at $j$ = 0.5 MA $cm^{-2}$ is 350 h, that is 7 times, 3.5 MA $cm^{-2}$ divided by 0.5 MA $cm^{-2}$ with $n = 1$, the nominal 50 h). Even if we assume an extremely aggressive void growth during the 'pre-damaging' phase and thus introduce an $n = 1.7$ such as actually determined from the data shown in Fig. 6.29a for the conditions in the 'pre-damaging' phase to the above proportionality calculation, the hypothetically degraded MTF would then be shown as the 'minus' signs in Fig. 6.30b.

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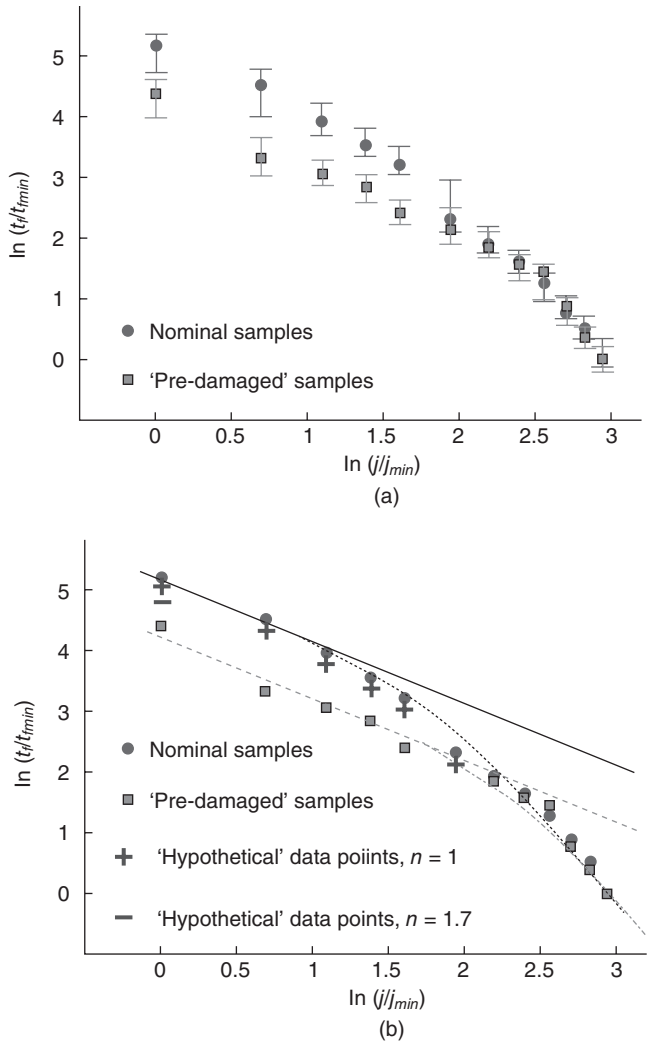


*6.30* Electromigration (EM) test results (Budiman *et al.*, 2010): (a) comparison between the nominal versus 'pre-damaged' samples, and (b) $n$ is principally 1 in both cases (the solid line for the nominal samples, and the dashed line for the 'pre-damaged' samples) but MTF tends to be depressed in the high $j$ range owing to extrinsic effects and thus deviating (the dotted line for the nominal samples, and the dashed-dotted line for the 'pre-damaged' samples) from the $n = 1$ trajectories; the 'hypothetical' data points (the 'plus' and 'minus' signs) indicate the shortened lifetime of the 'pre-damaged' samples if the 'pre-damaging' phase degrades the MTF more than its nominal 50 h owing to the very aggressive void growth.

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Evidently, there remains a significant gap with the MTFs of the second set of samples.

These data sets thus strongly indicate that Joule heating cannot act alone here in these Cu interconnect samples. In the range of $\ln j/j_{min} < 1.95$, the MTFs of the 'pre-damaged' samples (the square data points) are still significantly reduced from those of the nominal samples even after considering the shortened lifetime owing to the 'pre-damaging' phase (the 'plus' and 'minus' signs). Such a significant difference can be explained by electromigration-induced plasticity which introduces some permanent effects, perhaps in addition to the Joule heating effect. The significant difference here strongly suggests that the second set of samples have also suffered substantially higher electromigration fluxes than those of the first set of samples even though both were tested at the same low $j$, which further indicates there might be effects of a structural permanent difference between the two sets of samples. We believe that the high $j$ 'pre-damaging' phase for 50 h had created dislocation configurations at such high densities that they had accordingly aggravated the electromigration fluxes in the second set of samples beyond the nominal 50 h or even beyond the hypothetically degraded lifetimes owing to the aggressive/extremely aggressive void growth scenarios during the 'pre-damaging' phase.

Even though Joule heating is widely cited as the source of the deviation from $n = 1$ at high $j$, recent studies (Chang *et al*., 2003; Hau-Riege, 2006; Labun and Jagjitkumar, 2008; Wang *et al*., 2004; Wu *et al*., 2001) both experimentally as well computationally have shown that its effects on the global transport of atoms along the metal interconnect lines are somewhat modest. In the absence of extreme local instabilities (such as hot spots or local meltdown owing to current crowding effects, for instance), the effect of Joule heating is predicted to be merely a rise of between 5 and 10% at high $j$ compared with at low $j$ in the global temperature of the interconnect lines (Chang *et al*., 2003; Gurrum *et al*., 2008; Hau-Riege, 2006; Labun and Jagjitkumar, 2008; Wang *et al*., 2004; Wu *et al*., 2001). This is insufficient to cause a large drop in MTF at high $j$ that would be required to cause the $n$ to deviate from $n = 1$ line significantly. This is especially true for the case of the Cu–$SiO_2$ interconnect scheme, such as used in the present study, owing to the high thermal conductivity of $SiO_2$ (Wu *et al*., 2001). For the Cu–$SiO_2$ interconnect scheme, Wu *et al*. (2001) for instance using a combination of an analytical thermal model with a two-dimensional (2D) numerical simulation using the finite element method, has reported a less than 7% rise in global interconnect temperature at $j = 4.5$ MA cm$^{-2}$ compared with at $j = 0.5$ MA cm$^{-2}$ and, consequently, a factor of less than 2 in the MTF reduction owing to the temperature rise. The corresponding test conditions in the control data sets (i.e. the nominal samples) in the present study show at least a factor of 20 in the MTF reduction.

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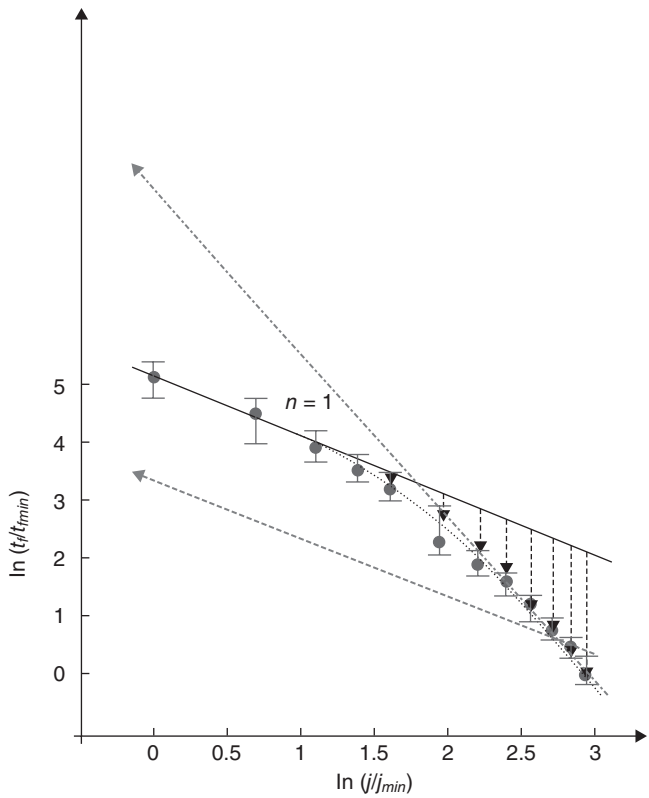
### 6.4.2 The danger of overestimating device lifetime

Finally, having recognized that any value of $n$ larger than one obtained from accelerated test conditions (i.e. high $j$ values) is the result of extrinsic effects, we reiterate the danger of overestimating device lifetime using the current methodology. If, for instance, we use the $n = 1.7$ as observed in the present study to extrapolate from the accelerated condition (high $j$) to the use condition (low $j$), that extrapolation would clearly lead to an overestimation of the device's actual lifetime (approximated by the actual MTF data point at low current density). This is illustrated by the dashed–dotted line in Fig. 6.31.




*6.31* Illustration of the impact of the current exponent ($n$) on the extrapolated lifetime. The danger of overestimation of device lifetime by using $n > 1$ is shown (dotted-dashed line), as is the more conservative extrapolation using $n = 1$ (dashed line), which is closer to the actual device lifetime in use conditions. Data from Fig. 6.29 is again used here for illustrative purposes.

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To improve the accuracy of the reliability assessment of devices under use conditions, we thus propose that the extrinsic effect has to be removed from the electromigration lifetime equation. This can be done simply by insisting on $n = 1$ in our lifetime assessment (illustrated by the dashed line in Fig. 6.31), which in most typical electromigration test conditions results in a more conservative prediction of device lifetime. This is true no matter whether Joule heating alone or, as we have proposed in the present study, electromigration-induced plasticity (in addition to Joule heating) is the root cause of deviation of MTF at high $j$ in the electromigration of Cu interconnects.

## 6.5 Conclusions and future trends

In studying the evolution of the microstructure in the Cu interconnects during electromigration using the synchrotron-based X-ray microdiffraction technique, we have unraveled a new phenomenon which has not so far been taken into consideration and which might thus change our current understanding of the electromigration degradation mechanisms. This unraveling of these plastic behaviors of copper polycrystalline lines undergoing high current density flux was made possible by the white-beam nature of the X-ray source used in the μSXRD technique. The current understanding of the electromigration phenomenon so far has only included the elastic response of the metallic grains against the global atomic migration in the interconnects. Our results show that this might not be the whole story as plasticity comes into the picture. Furthermore, when the extent of this plasticity is sufficiently high, this particular configuration could lead to enough additional electromigration flux to start changing the kinetics of the electromigration lifetime prediction. This would certainly have important industrial as well as fundamental implications. As advanced interconnect schemes push further and further into the nanometer regimes of the materials near their microstructural inhomogeneities, plasticity will continue to play significant roles in determining the overall responses of the devices under operational loading.

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# 7

# Scaling effects on electromigration reliability of copper interconnects

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**Abstract**: The effect of scaling on the electromigration (EM) reliability of Cu interconnects is investigated. First the intrinsic effect owing to scaling of the via and line dimensions is examined based on the dominant mass transport at the Cu top interface under EM. This is followed by a discussion of the extrinsic effects of processing-induced defects. EM results and failure modes are reviewed for both upstream and downstream electron flows, and the EM behaviors of multi-linked structures are discussed to further study the scaling effect. Methods of improving EM reliability are included and the results of using the CoWP cap are highlighted.

**Key words**: scaling, electromigration, Cu interconnect, cap layer, grain structure, failure mode.

## 7.1 Introduction

The scaling of Cu interconnects continues to drive the reduction in via/line dimension and barrier thickness, with a concurrent increase in the current density. This has rendered electromigration (EM) a serious reliability concern for Cu interconnects. Beyond the 45 nm technology node, Cu damascene structures have two basic EM reliability issues. First, the scaling down of the line dimensions inherently reduces the EM lifetime because less material is required to induce the EM failure even if the current density remains the same. Second, the ratio of the interface to the volume of the interconnect structure continues to increase with scaling. These two factors reduce the time required for damage formation for future technology nodes assuming that the diffusion at the cap layer interface dominates the mass transport under EM (Hu *et al.* 1999, 2006, Hau-Riege and Thompson 2001, von Glasow *et al.* 2003). Hu *et al.* (2004, 2006) proposed a geometrical model to predict the scaling effect on EM lifetime taking into account the reduction of the critical void size and the line dimensions. The scaling effect on the EM lifetime is shown in Fig. 7.1 as a function of the cross-sectional area of the Cu line for each technology node (Hu *et al.* 2006). The open circles



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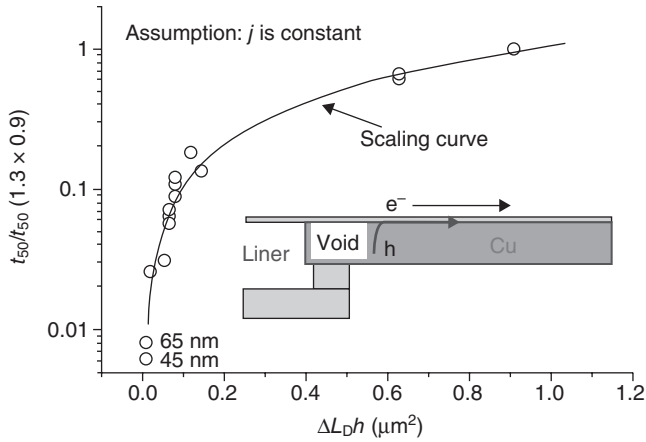


*7.1* Normalized EM lifetime as a function of $\Delta L_{cr}h$ (cross-sectional area *wh*) for various Cu interconnect generations (Hu *et al.* 2006).

are the experimental data points and the solid line is the modeling prediction. The model predicts that the EM lifetime decreases by half for each new technology node, assuming that the current density remains the same. This is in good agreement with the observed EM lifetime degradation with scaling starting at 1 μm line dimensions. Given the fact that the actual current density continues to scale up for each technology node, the EM lifetime continues to degrade with scaling.

In addition to the intrinsic effect of the dimensional scaling, there are extrinsic effects caused by processing-induced defects resulting from continuing interconnect scaling. In Cu interconnect, the vias connect the lower metal line to the upper metal line and are of particular concern as a weak link for reliability. The line/via structure with a high aspect ratio has been recognized as the most challenging issue for process integration. As the via dimensions shrink in each technology generation, both the via cross-sectional area and the surrounding barrier layer thickness are reduced. Processing difficulty in achieving thin and conformal barrier formation in via results in additional reliability issues arising from the barrier adhesion, integrity, and uniformity. In general, any defect at the via bottom can pose as a reliability weak point to limit the overall EM performance. In upstream EM tests, it is common to observe a bimodal EM lifetime distribution, in which the early failure mode (the weak mode) is caused by the void formation inside the via or at the via bottom (Fischer *et al.* 2002, Gill *et al.* 2002, Lee and Oates 2006, Lee *et al.* 2006, Li *et al.* 2004, Oates and Lee 2006). This failure mode is directly related to the via bottom processing, such as via etching, cleaning and barrier layer deposition. A slit-like void has been

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reported to form directly under the via bottom, resulting in an order of magnitude reduction in the EM lifetime (Lee and Oates 2006, Li *et al.* 2004, Oates and Lee 2006).

At the 65 nm node and beyond, with the Cu line width being scaled down below 90 nm, a polycrystalline grain structure or a mixture of bamboo and polycrystalline grain structures was reported (Hinode *et al.* 2001, Hu *et al.* 2007, Steinhogl *et al.* 2005, Zhang *et al.* 2007). Random line sections of polycrystalline grains were observed, especially at the trench bottom. In such Cu lines, the additional mass transport along the grain boundaries was found to further degrade the EM performance (Hu *et al.* 2007). As scaling continues, the surface-to-volume ratio of the Cu via and trench continues to increase, making it increasingly difficult to retain the bamboo-like grain structures. For future technology nodes, more small grains are to be expected in the Cu lines, making it increasingly important to understand the effect of the scaling grain structures on EM reliability of Cu interconnects.

In this chapter, we review the studies on the scaling effect on EM reliability of Cu interconnects. First, we describe the nature of mass transport under EM in Cu interconnects and deduce the scaling effect on EM lifetime for the standard Cu interconnect where the mass transport is dominated by diffusion at the cap interface. This is followed by a review of the experimental studies on EM reliability and the effects of interconnect scaling for both downstream and upstream current flows. Via scaling is shown to play a key role in controlling the void formation and the EM lifetime, particularly for the downstream current flow. For the upstream current flow, there are two failure modes caused by void formation in the trench or at the via, which are identified by different resistance traces and by failure analysis using transmission electron microscopy (TEM). In the third section, the experimental studies on the early failure under EM as an important reliability predictor at the chip level, are reviewed. A statistical methodology has been developed using multi-linked test structures to measure the contribution of the early failure to the EM lifetime statistics. This method has been applied to EM tests for both upstream and downstream electron flows. Two distinct failure modes are observed and their effects on EM lifetime and statistics are discussed. Finally, the recent development of the cap layer interface to improve EM reliability by reducing the interfacial mass transport is reviewed. The CoWP cap is found to be particularly effective for improving EM performance. The results from a recent study on the CoWP cap are summarized and its effect on EM reliability for future technology nodes is assessed. Looking ahead, with interfacial diffusion being suppressed, grain structure will become increasingly important in contributing to the mass transport and in impacting EM reliability. The implications for future technological developments will be discussed.

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## 7.2 Mass transport during electromigration (EM)

During EM, the atomic flux ($J_e$) driven by the EM driving force ($F_e$) can be written as:

$$J_e = nv_d \quad [7.1]$$

where $n$ is the atomic density and $v_d$ is the drift velocity. The drift velocity of the moving metal ions can be expressed as:

$$v_d = (D_{eff}/k_B T)F_e = D_{eff}Z^*_{eff}e\rho j/k_B T \quad [7.2]$$

where $D_{eff}$ is the effective diffusivity of the metal ions, $Z^*_{eff}e$ is the effective charge, $\rho$ is the metal resistivity, $k_B$ is the Boltzmann constant, and $T$ is the absolute temperature. Two parameters in equation [7.2] determine the drift velocity of metal ions and in turn the EM lifetime. The first is the current density $j$ which continues to increase with the line scaling as specified by the ITRS roadmap (http://www.itrs.net/reports.html). The second is the effective diffusivity $D_{eff}$ of moving ions along various diffusion pathways. In Cu damascene structures, mass transport can occur through several fast diffusion pathways including the Cu/SiCN cap interface, the Cu/Ta liner interface and the grain boundary. The relative contributions from these pathways can be assessed from their activation energies. Those energies have been measured for Cu interconnects to be 0.7–0.95 eV for grain boundaries (Gupta 1988, Surholt *et al.* 1994, Surholt and Herzig 1997), 0.8–1.1 eV for the Cu/SiCN interface (Fischer *et al.* 2002a, Hu *et al.* 2002, Tokogawa *et al.* 2002) and 0.7–1.8 eV for the Cu/Ta liner interface (Demuynck *et al.* 2004, Hu *et al.* 2003, Lin *et al.* 2002). By comparison, the diffusion through the Ta liner interface is small and can be ignored. Accordingly, the parameter $Z^*_{eff}D_{eff}$ can be expressed as:

$$Z^*_{eff}D_{eff} = Z^*_N D_N \delta_N/h + Z^*_{GB}D_{GB}\delta_{GB}f/d \quad [7.3]$$

where the subscripts identify the diffusion pathways by N as the Cu/SiCN interface and GB for grain boundary; $\delta$ is the width of the interface or the grain boundary, $d$ is the grain size, and $h$ is the line thickness. The parameter $f$ is a geometrical factor defined by the average orientation of the grain boundaries relative to the current flow. The parameters $f$ and $d$ are statistical in nature, depending on the grain structure in the Cu line. For small grain polycrystalline structures, there is a higher proportion of grain boundaries aligned with the current flow, so the value of $f/d$ is larger than the bamboo or near bamboo grains and contributes more to the mass transport. This is expected to be the case when the line width is scaled beyond the 65 nm node.

The EM lifetime is statistical in nature as it is related to the rate of damage formation at various flux divergence sites, which are statistically distributed. For simplicity, we consider a single damascene Cu line

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connected to a W via where the EM-induced void forms at the cathode end of the line. The EM lifetime $\tau$ can be written as (Hu *et al.* 2006):

$$\tau = \Delta L_{cr}/v_d \qquad [7.4]$$

where $\Delta L_{cr}$ is the critical void length to cause the line failure under EM, which is approximately the via size. If the mass transport is dominated by the diffusion along the Cu/SiCN interface and the grain boundary, the EM lifetime can be expressed as:

$$\tau = \frac{\Delta L_{cr} hkT}{e\rho j(D_N \delta_N Z_N^* + D_{GB}\delta_{GB} Z_{GB}^* fh/d)} \qquad [7.5]$$

For standard SiCN capped Cu interconnects with bamboo and near-bamboo grain structures, the parameter $f$ approaches zero and can be neglected, thus the EM mass transport is dominated by the Cu/SiCN interface diffusion, with little grain boundary contribution. In this case, $\tau$ is directly proportional to $\Delta L_{cr}h$ and inversely proportional to $j$. If the critical void size $\Delta L_{cr}$ is about the same as the line width $w$, $\tau$ would be scaled with $wh$, the cross-sectional area of the line, or $s^2$ with $s$ being the scaling factor. For each technology generation, the line dimensions are scaled by a factor of ~0.7, which yields a reduction of ~50% in the EM lifetime. This trend has been confirmed by Hu *et al.* (2006) for Cu interconnects with the SiCN cap interface, and the results are shown in Fig. 7.1. In the above discussion, the local Joule heating is assumed to be negligible for the current density $j$ used. In accelerated EM tests, the assumption may not hold; in that case, the $j$ dependence can be more than linear.

## 7.3 Effect of via scaling on EM reliability

In 7.2, the effect of scaling of the via dimensions was discussed and the result showed that the effect is significant in that the EM lifetime decreases by half for each subsequent technology generation for a constant current density. Although this describes the intrinsic geometrical effect of via scaling, via processing for dual damascene structures is most challenging owing to the difficulty of forming thin and conformal barriers in vias with high aspect ratio, particularly for Cu/low-$k$ interconnects. This raises a basic question concerning the effect of via processing in addition to the geometrical scaling on EM reliability.

A variety of test structures have been designed to study the EM lifetime and failure modes using either upstream electron flow (V1M2) or downstream electron flow (V1M1). Figure 7.2 shows the schematics of the test structures. Although the single-linked structures are used to study the basic failure mechanisms, multi-linked structures significantly increase the sample size, allowing the early failures to be observed. In this section, we discuss

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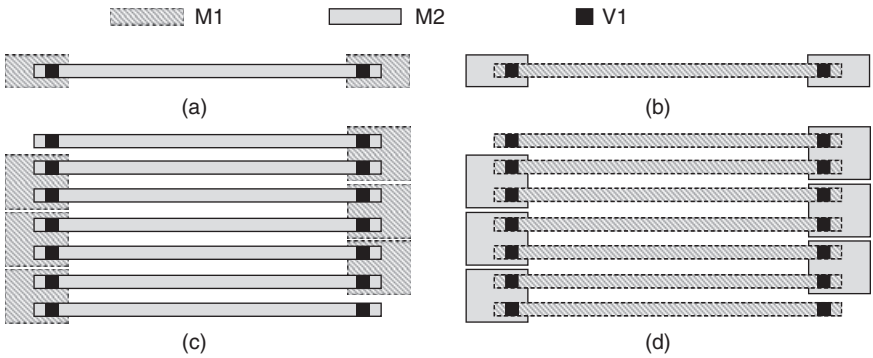
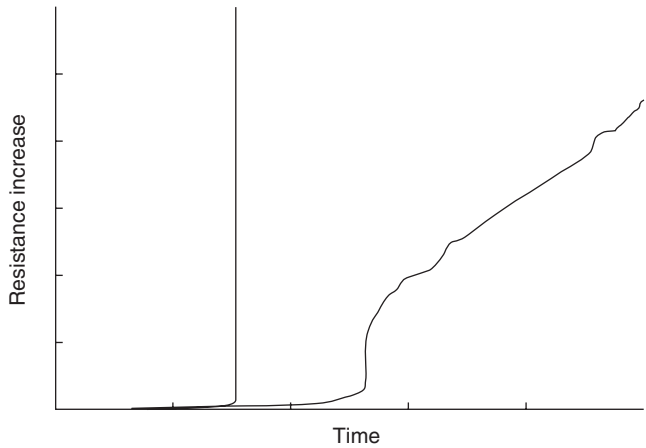



*7.2* Schematic of EM test structures: (a) single-linked upstream, V1M2; (b) single-linked downstream, V1M1; (c) multi-linked upstream, V1M2, $N$ = 10, 100; (d) multi-linked downstream, V1M1, $N$ = 10, 100.




*7.3* Progressive and abrupt resistance increases for typical single-linked downstream EM test structures.

the results using such test structures to investigate the via scaling effects on EM reliability for Cu/low-*k* dual damascene interconnects.

### 7.3.1 EM lifetime and failure mode with downstream electron flow

Stressing of single-linked EM structures with downstream electron flow from the upper to lower metal lines leads to either abrupt, large resistance increase or progressive monotonic resistance increases with the stress time. Typical examples are shown in Fig. 7.3. Examinations of the stressed vias

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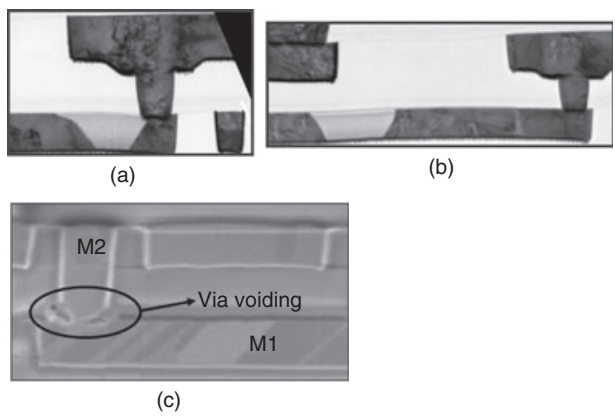
reveal that the progressive resistance increases are associated with voids that are located either (a) at the cathode via, extending along the line length direction, or (b) in the trench away from the cathode via, as shown in Fig. 7.4(a) and 7.4(b). In both cases, the trench liner maintains electrical redundancy at the point of void formation. The abrupt resistance changes, however, result from void formation directly under the vias, where the void is in the shape of a narrow slit, as shown in Fig. 7.4(c). The only variations in this failure mode seems to be the extension of the void in front of the via, and a small variation in the void depth below the via.

The various void locations can induce different critical failure void volumes, as shown in Fig. 7.4. If a void nucleates directly under the via, the effect of the line width on the EM lifetime are mediated through the scaling of the via size. This is confirmed by the downstream EM tests performed on single-linked M1 Cu lines with the line widths of 125 and 175 nm, where the M1 line width is the same as the V1 via size. Fig. 7.5 shows the EM test results, where the 175 nm lines exhibit a longer EM lifetime than the 125 nm lines. The EM lifetime was found to scale with the M1/V1 size, which can be attributed to the scaling of the critical void size $\Delta L_{cr}$. The failure mechanism is confirmed by focused ion beam (FIB) cross-sectioning analysis of failed samples. A typical large void under the via at the cathode end is observed (Fig. 7.6) where Cu atoms are completely depleted.

On the other hand, if a void starts to nucleate in the M1 trench away from the via, the scaling effects of the line width on the EM lifetime can be diminished. This is demonstrated in the EM test results of the single-linked V1M1 structures with different line widths of 60, 110, and 185 nm, as shown in Fig. 7.7. The cumulative distribution function (CDF) plots reveal that the




*7.4* TEM/FIB images of void formation for downstream electron flow: (a) at the cathode via, extending along the line direction; (b) in the trench away from the cathode via; (c) directly under the vias, where the void is in the shape of a narrow slit.

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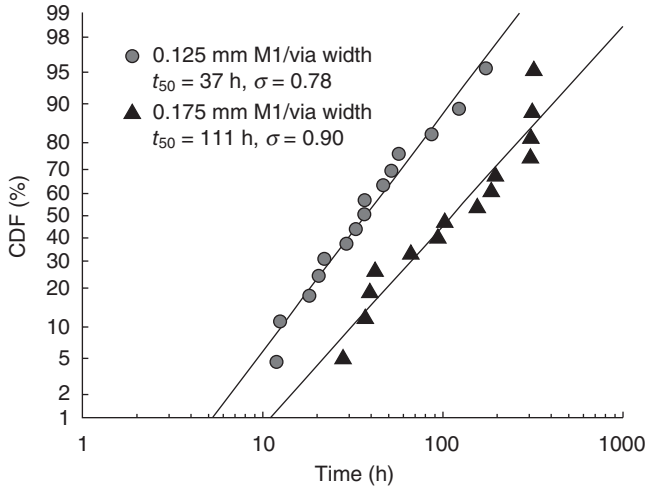
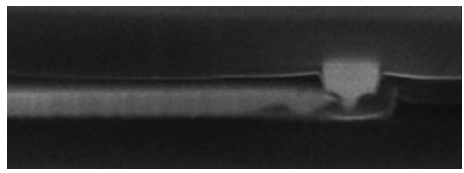
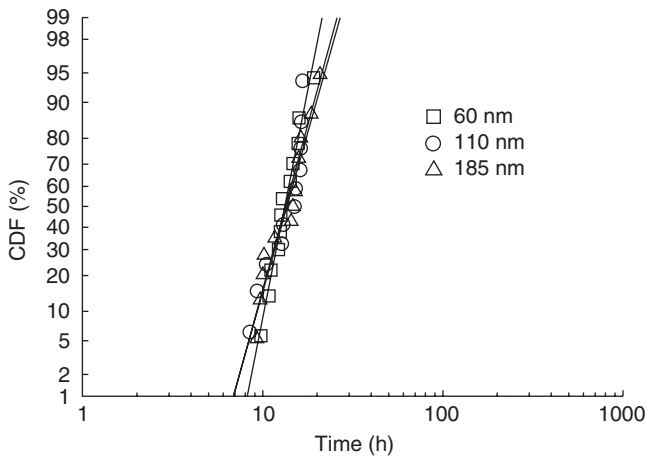



*7.5* CDF plots of single-linked downstream EM tests of 125 and 175 nm wide M1 lines. The EM tests were performed at $T = 270\,°C$, with $j = 1.0$ MA cm$^{-2}$.



*7.6* FIB image of one EM-failed sample in the downstream tests with the line width of 125 nm.




*7.7* CDF plots of single-linked downstream EM tests of M1 lines with different line widths. The EM tests were performed at $T = 300\,°C$, with $j = 1.0$ MA cm$^{-2}$.

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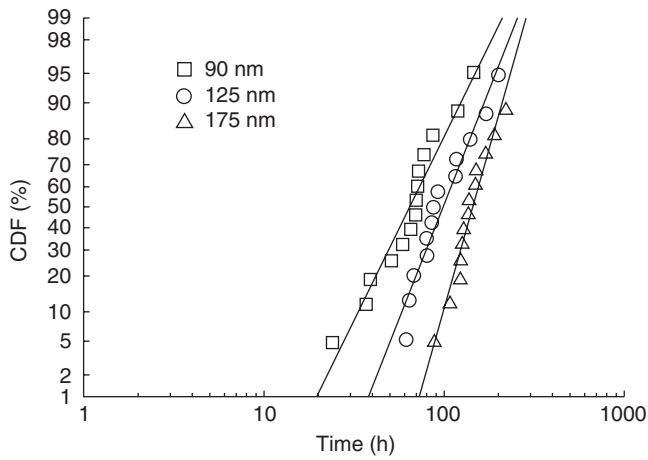
EM lifetime distribution is independent of the M1 line widths employed. The reasoning behind the line width independence is explained in the following. Because the void-induced EM failure is found to form in the M1 trench, the critical void size $\Delta L_{cr}$ remains constant, independent of the line width. The EM lifetime then depends solely on the metal line thickness $h$. Because the line thicknesses for test samples with different line widths are identical, the lifetimes become the same under the same temperature and current density conditions, as shown in Fig. 7.7.

## 7.3.2 EM lifetime and failure mode with upstream electron flow

The CDF plots obtained from the EM tests with upstream current flow are shown in Fig. 7.8 for three V1/M2 sizes of 90, 125, and 175 nm. In this study, all the line structures have the same cap layer interface and line thickness and are tested under the same conditions, thus the EM lifetime is expected to be directly correlated to $\Delta L_{cr}$. The line fails owing to void growth starting from the cathode end of the trench to span over the whole via. In this case, $\Delta L_{cr}$ is proportional to the via size and thus the EM lifetime should scale with the via width. This is in good agreement with the results shown in Fig. 7.8.

The resistance traces recorded during the EM test for the 125 nm test structures are plotted in Fig. 7.9. The resistance changes showed a typical intrinsic EM failure behavior where the first abrupt resistance increase




*7.8* CDF plots of single-linked upstream EM tests of 90, 125 and 175 nm wide M2 lines. EM tests were performed at $T = 330\,°C$, with $j = 1.0$ MA cm$^{-2}$.

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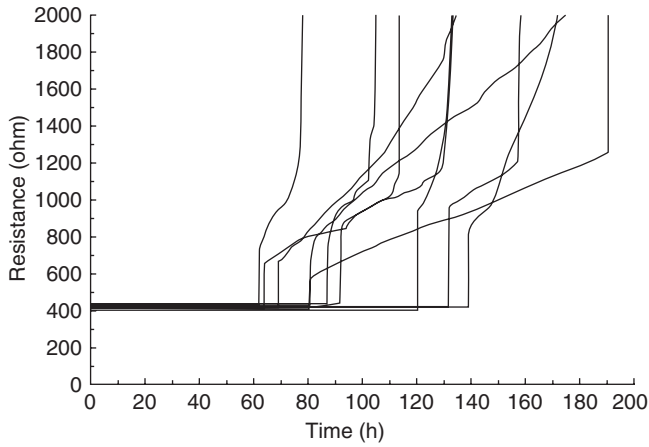
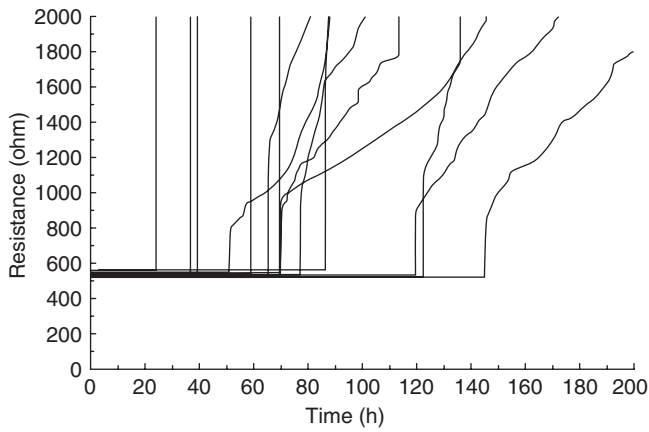



*7.9* Resistance traces of the 125 nm wide EM samples in the upstream EM tests.




*7.10* Resistance traces of the 90 nm wide EM samples in the upstream EM tests.

occurs when a void growing from the cathode end covers the whole via. The current is then shunted to the Ta barrier, causing the resistance to abruptly increase. The subsequent gradual increase in resistance is the result of continuing void growth along the M2 trench. When the Ta barrier can no longer sustain the current density, the barrier burns out to cause a final abrupt increase in resistance.

In contrast, the resistance traces for the 90 nm wide lines exhibited both gradual and abrupt increases as shown in Fig. 7.10. The abrupt resistance increase is attributed to either via bottom voiding or trench voiding caused by extrinsic process-induced defects. The gradual increase is attributed to

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*7.11* FIB image showing a large cathode void in M2 trench for one EM failed 125 nm wide Cu line.

the same intrinsic failure mode as described for the 125 nm lines. The combination of the two failure modes leads to a wider lifetime distribution for the 90 nm lines than the 125 and 175 nm lines, as shown in Fig. 7.8.

One of the 125 nm wide EM-failed samples is analyzed using FIB, and the image is shown in Fig. 7.11. Even though the via structure cannot be clearly discerned owing to severe joule heating, a large trench void at the cathode end is evident. This damage mode supports the intrinsic failure mechanism owing to void formation at the cathode driven by interfacial mass transport. This is also consistent with the resistance traces shown in Fig. 7.9.

## 7.4 Multi-linked statistical tests for via reliability

The previous discussion was focused on the EM tests performed on the single-linked EM test structures. Both types of resistance increases, abrupt and progressive changes, are observed in the single-linked structures. To assess the EM reliability at the chip level where millions of Cu lines are connected, it is essential to develop a method to determine the rate of the early failures. For this purpose, multi-linked test structures are designed for measuring the early failure statistics and two examples of multi-linked test structures for upstream and downstream current flow are shown in Fig. 7.2(c) and 7.2(d). In EM tests, multi-linked test structures with different number of links, $N = 1$, 10 and 100 for example, are used for statistical determination of different failure modes. The multi-linked structures greatly increase the number of test structures and thus significantly increase the probability of detecting the early failures.

The multi-linked test structures are designed for quantitative data analysis to determine the proportions of the failure modes and EM statistics. The analysis is based on the 'weakest link approximation' (WLA) statistics in combination with the Monte Carlo simulation (Lee *et al.* 2004, Ogawa *et al.* 2001). This method has been applied to study the scaling effect on via reliability with the upstream electron flow. The CDF plots of the upstream multi-linked structures with $N = 1$, 10, and 100 from the experiments and the subsequent weakest link approximation (WLA) Monte Carlo simulation are presented in Fig. 7.12 as a function of the line width. Solid symbols

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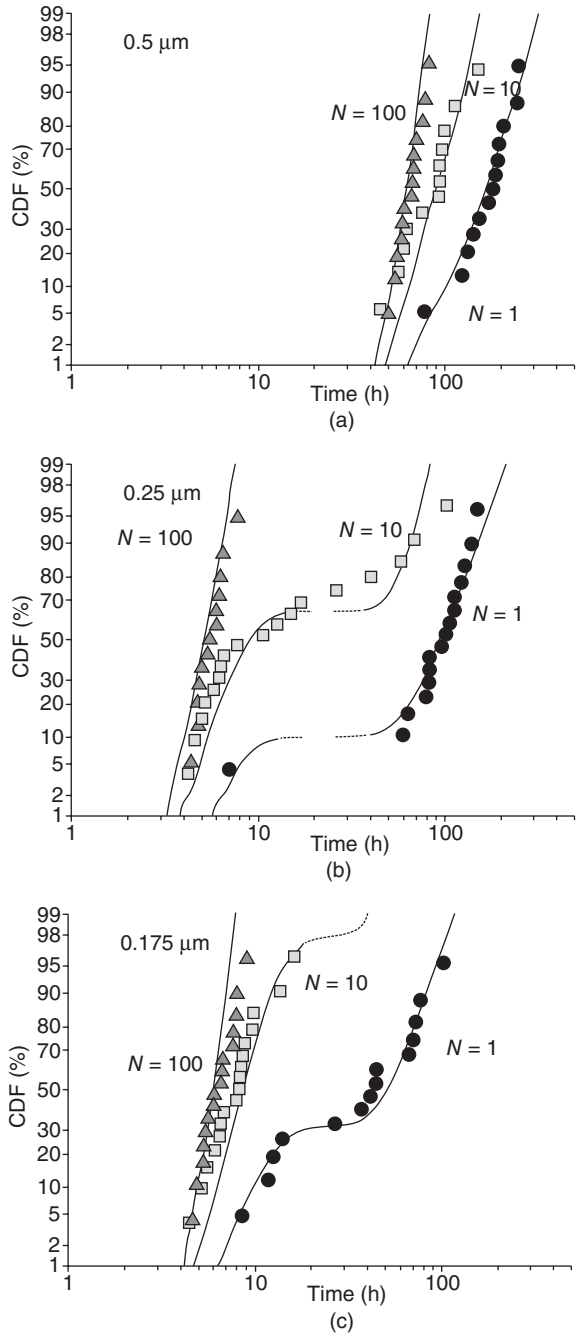


*7.12* CDF plots of upstream EM test structures as a function of the line width of (a) 0.5 μm, (b) 0.25 μm, and (c) 0.175 μm. Solid symbols are the real lifetime data and small dotted lines are generated by WLA Monte Carlo simulation. EM tests were performed at $T = 325\,°C$, with $j = 1.0\ \text{MA cm}^{-2}$.

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*Table 7.1* Summary of EM lifetime data for upstream M2 electron flows. EM tests were performed at $T = 325\,°C$ and $j = 1.0$ MA cm$^{-2}$

| Line width (μm) | 0.5 | 0.25 | 0.175 |
|---|---|---|---|
| Percentage of weak mode (%) | 15 | 10 | 30 |
| $t_{50}$ of weak mode (h) | 90 | 8 | 11 |
| $\sigma$ of weak mode | 0.25 | 0.3 | 0.3 |
| $t_{50}$ of strong mode (h) | 180 | 100 | 60 |
| $\sigma$ of strong mode | 0.25 | 0.35 | 0.3 |

are the actual lifetime data from the experiment and the lines with small dots represent the results generated by Monte Carlo simulations. The branching caused by the bimodal failure mechanism in the data is readily observed for both the 0.25 μm and the 0.175 μm structures. With the Monte Carlo simulation for the best fitting curves based on the WLA, even the results of the 0.5 μm structures reveal both the strong failure and the weak failure modes. Together with the simulations, the average lifetime $t_{50}$, standard deviation $\sigma$, and the failure population for the strong and the weak modes can be determined and the results are listed in Table 7.1. The EM lifetime of the intrinsic strong mode shows a systematic linear decrease with the line width scaling. This can be attributed to the decrease of the critical void size with line/via width as discussed above. It is interesting to note that the weak via-related failure mode lifetimes are not simply related to the change of the line width; instead, they are more closely related to the extrinsic process-induced defects, such as poor barrier coverage at the via bottom. As the linewidth decreases, processing control becomes more difficult and challenging. This is reflected in the increase of the proportion of the weak mode and the decrease in the lifetime of the weak mode for the 0.25 and 0.175 μm test structures.

## 7.5 Methods to improve the EM lifetime

The reliability concern for Cu interconnects with scaling has generated significant interest recently in developing methods for improving the EM reliability. These include the use of Cu surface alloying, the formation of a CuSiN top layer, and the formation of a metal cap layer underneath the SiCN passivation layer. The use of a metal cap layer, such as CoWP, CuSnP, Pd, Ta and Ru, was found to be most effective in suppressing the cap interface diffusion. Figure 7.13 compares the CDF plots of the downstream EM tests for Cu interconnects with SiCN cap and CoWP cap. The test structures are fabricated by using the 45 nm technology process with test line width of 80 nm and line height of 144 nm. The EM results show that compared with the SiCN cap, the CoWP cap improves the EM lifetime of the Cu

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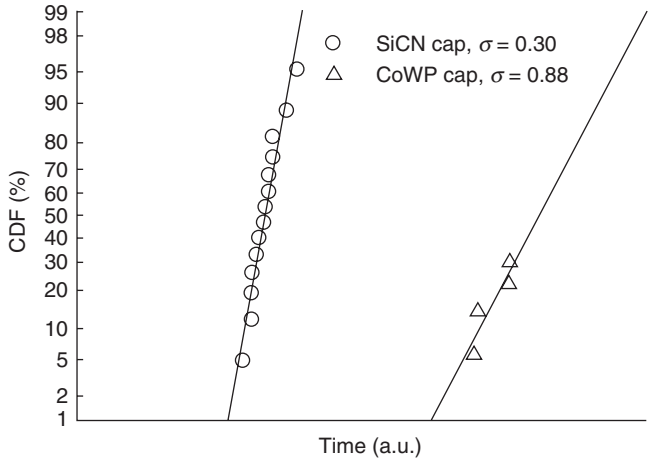


*7.13* CDF plots of the M2 Cu interconnects with different caps: SiCN versus CoWP. EM tests were performed at $T = 330\,°C$, with $j = 1.0$ MA cm$^{-2}$.

interconnects by ~160 times with an increase in $\sigma$ from 0.30 to 0.88. Only four of the CoWP capped Cu lines failed when the test was terminated even after a long period of current stressing. The improvement of the EM lifetime for the CoWP cap is the result of the reduction in the Cu/cap interface diffusion, which can be attributed to the highly ordered crystalline interface between Cu and CoWP (Meyer and Zschech 2007), as well as the much higher bonding strength between Cu and Co compared with that between Cu and amorphous SiCN (Lane *et al.* 2003). The difference in the interface crystalline quality is demonstrated in Fig. 7.14 using high-resolution TEM (HR-TEM) analysis along the Cu/SiCN and Cu/CoWP interfaces. It can be seen that the Cu line has a sharp interface with the SiCN cap, which has no distinct crystalline features. In contrast, for the Cu/CoWP interface, almost perfect crystalline planes of Cu extend all the way through the CoWP metal cap with no distinguishable interface in between. This indicates that the Cu/CoWP interface is characterized by highly ordered crystalline structures with strong bonding strength to suppress the interface diffusion.

Failure analyses by FIB and TEM observations show that for the SiCN-capped Cu lines, voids form either at the cathode via corner extending along the Cu line direction, or in the trench a certain distance away from the cathode via. For the SiCN capped lines, different failure locations show corresponding resistance changes: via corner voiding corresponds to a relatively small initial resistance increase, whereas the trench voiding corresponds to a large initial resistance change, as shown in Fig. 7.15 and 7.16. In comparison, for the CoWP capped Cu lines, voids mostly form in the

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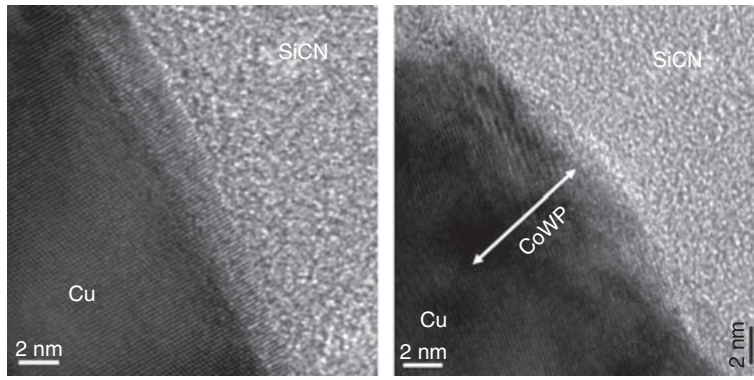
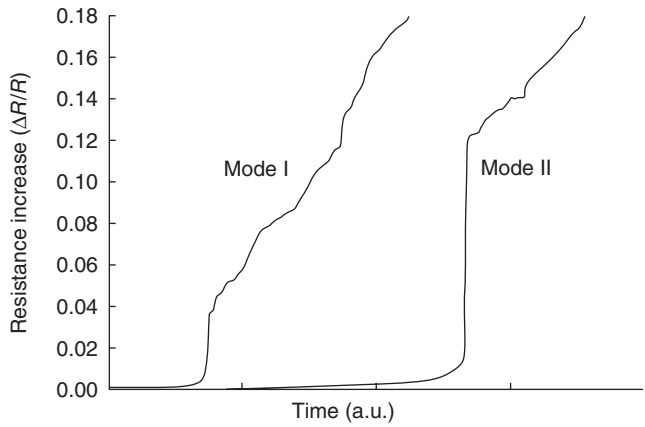



*7.14* High-resolution TEM images of different Cu/cap interfaces: (a) Cu/SiCN, (b) Cu/CoWP/SiCN.




*7.15* Typical resistance traces of mode I and mode II failures: mode I with a small initial resistance increase and mode II with a large initial resistance jump.

trench away from the cathode via, irrespective of the amount of the initial resistance step, as shown in Fig. 7.17. The difference in the voiding locations for these two cap layers can be attributed to the difference of the interface diffusion. For the SiCN cap, the cap interface diffusivity is large, so voids can move readily along the interface and eventually accumulate at the cathode via corner to fail the line. In contrast, for the CoWP capped Cu lines with interface diffusion effectively suppressed, voids can easily get trapped at locations with either an interface defect or a large grain triple junction. The trapped voids grow in the trench away from the cathode via, eventually causing the line to fail under EM.

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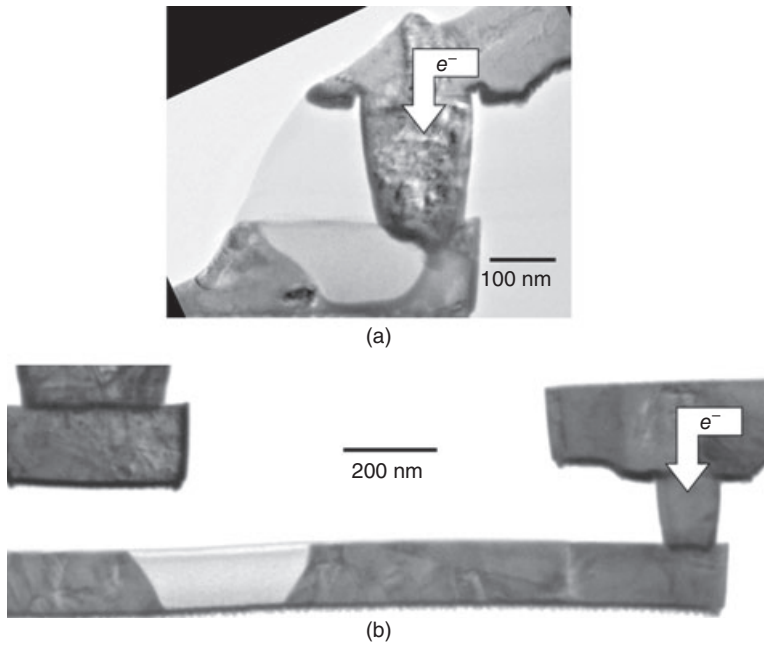
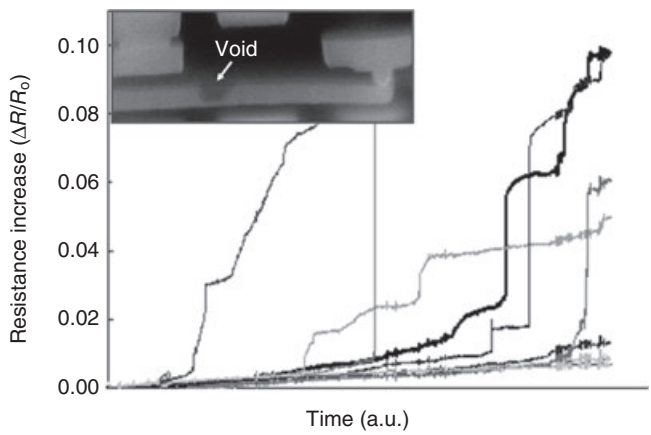



*7.16* Cross-sectional TEM images of EM failed samples showing different voiding locations: (a) at the via corner; (b) in the trench away from the via, corresponding to mode I and mode II failures in Fig. 7.15, respectively.




*7.17* Normalized resistance traces (R-trace) for large grain and CoWP capped samples, FIB image showing void formation in the trench away from the cathode via.

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## 7.6 Conclusion and future trends

In this chapter, we have discussed the via scaling effects on EM reliability for Cu interconnects. First we examined the intrinsic effect of scaling of the via and line dimensions based on the dominant interface mass transport under EM. The intrinsic effect was found to be significant, resulting in a decrease of EM lifetime by half for each technology node even with a constant current density. This was followed by a discussion of the extrinsic effects of processing-induced defects which were traced to the difficulty of processing the dual damascene structure. Such defects can significantly degrade the EM lifetime and statistics. To investigate the via scaling effects, a variety of test structures were designed, including single-linked and multi-linked structures. EM test results and the characteristics of the failure modes are discussed for both upstream and downstream electron flows. Finally, we summarized the method of using a metal cap layer to improve EM reliability and highlighted the results of the CoWP capping layer.

To conclude this chapter, we examine the scaling effect by projecting the EM performance for the CoWP technology. For this purpose, the EM lifetime is expressed as:

$$\tau = \frac{\Delta L_{cr}}{v_d} = \frac{\Delta L_{cr} kT}{e\rho j(Z_N^* D_N \delta_N / h + Z_{GB}^* D_{GB} \delta_{GB} / d)} = \frac{\Delta L_{cr} hkT}{Z_N^* D_N \delta_N e\rho j(1 + fgh/d)} \quad [7.6]$$

The $g$ factor, defined as the ratio of the mass transport through the grain boundary vs. the cap interface, can be expressed as:

$$g = Z_{GB}^* D_{GB} \delta_{GB} / Z_N^* D_N \delta_N \quad [7.7]$$

Equation [7.6] is written in a format to facilitate the discussion of cap layer and grain structure effects on EM lifetime. According to equation [7.6] and the model proposed by Hu *et al.* (2006), the ratio of the median lifetime for each technology node relative to that of the 0.13 μm technology is plotted in Fig. 7.18 as a function of the critical void volume $\Delta L_{cr} h$ (or the cross-sectional area $wh$). Both grain boundary and interfacial diffusion contributions to mass transport are included here. For standard SiCN capped Cu interconnects with bamboo or near-bamboo microstructures, the $f$ term approaches to zero and can be neglected, thus the EM mass transport is primarily controlled by diffusion at the Cu/SiCN interface. For each technology node, if we assume the current density $j$ remains the same, the EM lifetime degrades by half owing to the scaling of the geometrical factor

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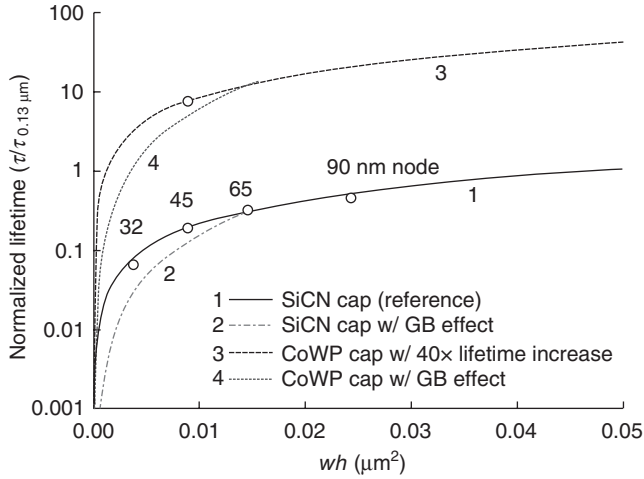


*7.18* Normalized EM median lifetime versus *wh* (cross-sectional area) for various Cu interconnect generations considering different dominant Cu diffusion paths. The data points of open circle are experimental data based on this study and the results provided by GLOBALFOUNDRIES.

$\Delta L_{cr}h$ ($wh$), as shown by the reference line '1' in Fig. 7.18. However, when the CoWP metal cap is used, the atomic diffusion along the interface is significantly suppressed, resulting in a reduction of $D_N$ by a factor of 40~160 depending on the metal cap process (Zhang *et al.* 2010). The scaling curve shifts up significantly as shown by line 3 in Fig. 7.18, where we assume a 40× lifetime improvement for demonstration.

As scaling continues, more small grains emerge in the Cu lines after the 65 nm node, and a higher proportion of grain boundaries are aligned with the current flow. This causes an increase in $f$ with a smaller $d$, resulting in an overall increase of the $fgh/d$ term. Thus, the grain boundary diffusion becomes increasingly important, which, in turn, accelerates the mass transport under EM and degrades the EM performance, as illustrated by the dashed line labeled as '2' in Fig. 7.18. The presence of small grains can have a larger impact on the EM lifetime for structures with CoWP capping, as reported by Zhang *et al.* (2010). This is because the suppression of interfacial diffusion by the CoWP cap causes the grain boundary diffusion to become more dominant in controlling the mass transport. Consequently, a small change in the grain structure can yield a large change in the overall Cu diffusivity as well as the EM lifetime. Nevertheless, the benefit of the CoWP cap over the SiCN cap remains significant even for the 32 nm technology node, as evidenced by comparing line 2 and line 4. To ensure EM

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reliability for the 22 nm technology node and beyond, the grain structure must be optimized together with the cap layer process.

In the above estimate of the scaling effect, we use a simple approach by treating the effect of the grain structure on EM lifetime as an average of the grain size and orientation. In reality, the problem is considerably more complicated and inherently statistical in nature. This can be seen from the results shown in Fig. 7.13 where the standard deviation $\sigma$ increases from 0.30 for the SiCN cap to 0.88 for the CoWP cap for the same Cu grain structure. This suggests that the EM characteristics, particularly its statistics, depend not only on the average grain structure but also on the coupling between the mass transport along the grain boundary and the cap interface in forming the voids which lead to the EM failure. This raises interesting questions for future studies.

## 7.7 Acknowledgements

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# 8

# Electromigration failure in nanoscale copper interconnects

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**Abstract**: An introductory discussion is presented to provide specific context to understand reliability trending as nanoscale dimensions (tens of nm) for advanced complementary metal oxide semiconductor (CMOS) technology become ubiquitous, i.e., not just at the transistor gate. There are three main sections: (1) process solutions being developed for Cu interconnects; (2) improving electromigration (EM) margin of Cu-based interconnects; and (3) microstructure effects on EM reliability. Finally, some discussion beyond the use of the canonical Cu interconnect are discussed.

**Key words**: electromigration, copper interconnects, metal capping, microstructure, nanoscale COMS technology.

## 8.1 Process solutions being developed for copper interconnects

### 8.1.1 Introduction to copper-based interconnect technology

There is perhaps some irony in the fact that 'interconnects', consisting of the metallization and surrounding dielectrics that route all electrical signals within advanced microchips, are most appreciated when they do essentially nothing (at least to the naked eye). An interconnect's primary function is to connect an electrical output to another electrical input, all at chip level, and vice versa, and as long as such interconnects transmit electrical signals without loss of fidelity and with minimal latency or supply electrical bias without detrimental power loss, then microelectronics devices should only be functionally limited by the behavior of the transistors that make up the bulk of the active circuitry within a given microchip. More realistically, however, functionally passive metallization does not behave so passively at the atomic scale, and its consequences can be significant. Metal atoms within interconnects jostle about under the action of external forces and, if long enough times are sampled, the nanoscopic movements of these atoms can be microscopic enough to lead to macroscopic device failure. The movement of metal ions under the influence of some driving force has several manifestations that lead to interconnect failure. Such failure mechanisms include stress-migration (metal void-generated electrical contact failures



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under thermomechanical stress), metallic corrosion shorting (interaction of metals with corrosive ambient and residual electrical bias present during processing), and metallic bridging under electrical stress owing to metal ionic drift into the adjacent interconnect dielectric (leading to dielectric breakdown between adjacent metals during electrical stress).

Electromigration (EM), that is metal void-generated contact failures under applied electrical current, is probably the most well-known interconnect failure mechanism and has been both an important topic in reliability physics and a key reliability metric for robust process technology development since the mid-1960s (Blech and Sello, 1966; d'Heurle and Ho, 1978; Ho and Kwok, 1989; Kwok, 1993; Hu *et al.*, 1995; Clement, 2001). During EM, the application of current through a metal creates the so-called 'electron wind' and causes metal ions to hop in aggregate from lattice site to lattice site along the direction of electron flow from the cathode end (the electron source side) to anode end. The continued flow of these metal ions from a given site can eventually trigger void nucleation and subsequent void growth. The void growth can then lead to interconnect failure by open circuit. This classical representation of EM is necessary to understand EM for advanced interconnect applications; however, a more nuanced picture of EM will be needed to understand the potential reliability trends for advanced Cu interconnects beyond 32 nm node.

During the earlier era of microelectronics, spanning from the mid-1960s to 1997, Al-based metallization was the primary metallization used to form the interconnections between transistor elements within a microelectronic device such as a microprocessor. Starting around 1997, Cu-based metallization was introduced to enable the necessary performance scaling (Edelstein *et al.*, 1997). Because Cu metallization became the new manufacturing process for advanced interconnects, much refinement in the basic Cu integration process has been done to improve on interconnect defectivity and uniformity so that technology scaling can continue at least up to the year 2015 (ITRS, 2009) before new solutions must be developed to keep pace with scaling requirements. Furthermore, tweaks to the basic Cu process and integration approach have been developed to improve either interconnect performance and/or reliability. These improvements have a direct bearing on EM performance and, in this chapter, we attempt to assess how EM performance might be expected to trend for the remainder of this decade.

### 8.1.2 The canonical copper interconnect and technology scaling

The canonical or standard picture of a Cu interconnect used in advanced CMOS-based technology appears little changed from its first use around 1997 (Edelstein *et al.*, 1997; Li *et al.*, 2004) and is depicted in Fig. 8.1.

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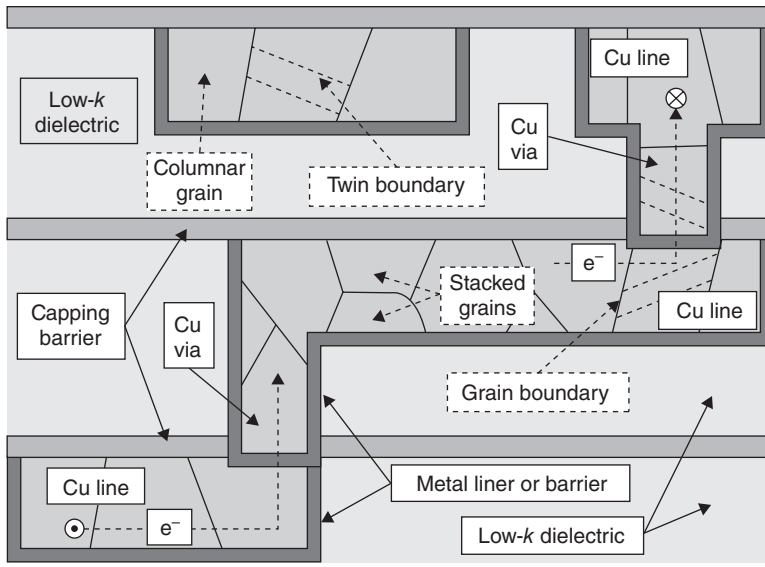


*8.1* Cross-sections of a dual-damascene interconnect structure in advanced Cu-based interconnects since 130 nm node, including lower trench, connecting via, intermediate interconnect, next level via and trench. Each trench feature is surrounded by diffusion barriers, on the bottom and sidewalls by a Ta-based metallization and on the top by a capping dielectric. In between the layers of interconnect metal is usually a low-*k* dielectric; this and the capping dielectric are in continual need of replacement to lower-*k* dielectric as technology scaling continues, but doing so is a great challenge for process and integration engineering. The Cu metallization within the trench consists of multiple grains along the interconnect length. Some segments can contain more than one grain along the width or height directions. Cu grains are also prone to 'twinning'. Finally, the electron flow during EM is also depicted. The circle with dot within it and circle with 'X' within it represent out-of-page and into-page directions, respectively.

Interconnects are fabricated using a so-called 'damascene' approach, where a blanket film dielectric on a Si wafer is patterned and etched to form open spaces (trench and via openings). Via openings, for connection to the metal level immediately below, are made either before or after a trench pattern is created. Cu metallization is deposited within the trench and via features using electrochemical deposition (ECD). Before such Cu deposition, however, a metal diffusion barrier, typically Ta-based, and Cu seed layer must be deposited, using physical vapor deposition, to enable conformal growth of Cu metallization during an ECD plating process. Good quality metal diffusion barrier is needed to keep any Cu from 'out-diffusing' into the low-*k* dielectric (Michael *et al.*, 2003a, 2003b; Augur *et al.*, 2003; Lu

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*et al.*, 2005; Pyun *et al.*, 2005) and potentially allowing the dielectric to be shorted out under electrical bias, since Cu is known to be a ready diffuser into such dielectrics under electrical bias (Tsu *et al.*, 2000), if pin hole defects exist within the metal barrier. After out-diffusion, the Cu then subsequently oxidizes within the inter-metal dielectric (Michael *et al.*, 2003a, 2003b). The Cu plating creates a blanket film overburden above the trench feature that needs to be removed by chemical mechanical polishing (CMP) to eventually form the metal interconnect. CMP flattens or 'planarizes' the trench top surface for subsequent capping by a dielectric diffusion barrier. The Cu microstructure is usually improved and stabilized somewhat (increased grain size and stabilized Cu grain texture) by use of a thermal anneal treatment (Hu *et al.*, 2007b) with overburden present or maybe after overburden removal by CMP, depending on the integration approach used.

Overburden anneal is usually preferred, however, because it minimizes the potential for void generation within the interconnect or hillock formation on the trench surface during anneal. The overburden presence also allows microstructure evolution during anneal from the overburden to penetrate into the trench feature and improve the resulting trench microstructure (Harper *et al.*, 1999; Lingk and Gross, 1998; van den Boom *et al.*, 2007), at least for interconnects greater than 250 nm in width. Following CMP, a dielectric film, typically a form of $SiC_xN_y$ in presently available 90, 65, and maybe 45 nm technology nodes, covers or 'caps' the remaining free Cu surface so that Cu is fully confined within its trench by diffusion barriers. The dielectric cap layer can also function as an etch stop during via etch when a metal layer above must be connected to a metal layer below.

A procedure whereby such via are formed in conjunction with trench formation above is known as a 'dual-damascene' integration scheme where metal barrier/Cu-seed/Cu-plating steps are subsequently carried out into both via and trench concurrently. Typically, the first Back-end-of-Line (BeoL) metal layer, generally called 'M1', is made using a 'single damascene' integration scheme for connection to a lower tungsten (W) contact plug and eventual connection to transistors or Si substrate. At M2, a dual damascene process is used to connect to the M1 interconnect. This dual-damascene process is then repeated level-by-level until the complete metallization stack is generated. Generally, the interconnect feature size (width and often length) at lower or intermediate metal level is at or near the minimum allowable critical dimensions at a given technology node. The interconnect dimensions at the upper metal level tend to be larger, especially at the highest metal levels, where power and signal routing are used and finally where bond pad connections for access to device package wiring or solder bumping are needed. Thus, the interconnect layout tends to be 'hierarchical' in the sense that lower level interconnect dimensions tend to be smaller than those found toward the top levels; however, such dimen-

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sional transitions and the extent of such hierarchy are entirely dependent upon product type, cost, performance, and potential reliability issues that are not specifically related to EM.

### 8.1.3 Issues and evolution of the canonical copper interconnect

The 'canonical Cu interconnect' model above has not, however, stayed constant with time because its evolution is needed to keep pace with pressing technology needs. Manufacturing feasibility at a given point in time is an important consideration because the ITRS roadmap has required several adjustments to the rate of implementation of low-*k* dielectrics because of difficulties encountered incorporating them into a high yielding manufacturing process (Shaviv, 2008; Gambino, 2008; Lu, 2009). Although the overall integration scheme is pretty much the same, a number of improvements have occurred since Cu was first introduced. The intra- and inter-metal effective dielectric constant has decreased owing to new materials substitutions such as $SiC_xO_yH_z$ (carbon-doped oxide; $k \sim 2.9$) for fluorinated silica glass (FSG; $k \sim 3.5$), which replaced tetraethyl orthosilicate (TEOS; $k \sim 4.0$) and capping dielectric $SiC_xN_y$ ($k \leq 6$) for $SiN_x$ ($k > 6$). Etch and CMP processes have evolved for better overall uniformity across a Si wafer and for addressing differences in metal density and feature size. The dielectric cap process has been gradually improved through utilization of surface pretreatments and time-window management before capping dielectric deposition for better adhesion/mechanical strength, EM performance, and corrosion prevention. The barrier metal has been gradually thinned in each generation to reduce the overall interconnect resistivity. Additional changes for more advanced technologies are also pending. Somewhere before the 15 nm node, ultra low-*k* porous interconnect dielectrics ($k \leq 2.5$), EM mitigation process enhancements (such as metal capping, alloying, and/or interface treatment), and possibly atomic layer deposition (ALD) barriers will be implemented, provided that they are proven to be suitable for large-scale manufacturing (van Roosmalen, 2006). Beyond 15 nm, the inherent difficulty in mitigating the progressively worsened resistivity of Cu metallization while simultaneously placing increased demands on the process margin and performance poses a formidable challenge. Table 8.1 shows how the maximum current density, resistivity, and metal barrier thickness might be expected to scale down to the 7 nm node. Whereas other trends found in the ITRS roadmap are also very important, these three items are of particular interest to EM reliability, although, for brevity, the matter of barrier thickness scaling is only touched upon in this chapter (Traving *et al.*, 2004).

A significant increase in resistivity from both grain boundary and interface electron scattering has been well-characterized by multiple authors

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*Table 8.1* ITRS values used to predict EM drift velocities at each technology node

| Interconnect half-pitch $w$[a] (nm) | $j_{max,ITRS}$ ($T$ = 105 °C), for intermediate wire (MA cm$^{-2}$) | $\rho_{Cu,ITRS}$ ($T$ = 105 °C) (μΩ cm) | M1: Cu metal barrier thickness (nm) |
|---|---|---|---|
| 130[b] | 1.1 | 2.2 | 14.00 |
| 90[c] | 0.891 | 3.15 | 6.50 |
| 65[d] | 0.995 | 3.51 | 5.20 |
| 45 | 1.44 | 4.08 | 3.30 |
| 32 | 2.10 | 4.98 | 2.61 |
| 22 | 2.97 | 6.43 | 1.96 |
| 15 | 4.13 | 8.10 | 1.30 |
| 10 | 5.92 | 11.25 | 0.95 |
| 7 | 7.96 | 14.06 | 0.70 |

Note: [a]From ITRS (2001, 2005, 2007, and, primarily, 2009; [b]From ITRS (2001); [c]From ITRS (2005); [d]From ITRS (2007).

(Besling *et al.*, 2004; Gignac *et al.*, 2007; Im *et al.*, 2005; Kim *et al.*, 2003; Rossnagel and Kuan, 2004; Shimada *et al.*, 2006; Steinhögl *et al.*, 2002, 2004, 2005; Sun *et al.*, 2009; Tay *et al.*, 2005; Wada *et al.*, 2009; Yarimbiyik *et al.*, 2006; Zhang *et al.*, 2004a, 2004b) to the point that their respective interconnect delay contributions are well-predicted in the ITRS roadmap for the rest of this decade. In Fig. 8.2, Cu interconnect resistivity as a function of the technology node is shown along with data from some representative authors. The resistivity contributions are modeled using the formalism developed by Steinhögl *et al.* (2002, 2004, 2005), and the primary drivers for interconnect resistivity increase are shown to come from grain boundary (Mayadas and Shatzkes, 1970) and surface (interface) scattering (Fuchs, 1938; Sondheimer, 1952). The form provided by Steinhögl *et al.* (2002, 2004, 2005) is as follows:

$$\rho = \rho_0 \left\{ \frac{1/3}{\left[\frac{1}{3} - \frac{\alpha}{2} + \alpha^2 - \alpha^3 \ln\left(1 + \frac{1}{\alpha}\right)\right]} + \frac{3}{8} C (1-p) \left(\frac{1+AR}{AR}\right)\left(\frac{\lambda}{w}\right) \right\} \qquad [8.1]$$

where $\alpha = \left(\frac{\lambda}{d_{gb}}\right)\left(\frac{R}{1-R}\right)$, $w$ is the width, $AR$ the aspect ratio (height over width), $\rho_0$ the bulk material resistivity, $\lambda$ the mean free path, $d_{gb}$ the average distance between grain boundaries, $p$ the specularity parameter at the metal surface, and $R$ the grain boundary reflectivity coefficient. The parameter $C$ is a constant and equals 1.2 for rectangular cross-sections. Equation [8.1] is an approximation to the exact solution of the transport problem in a con-

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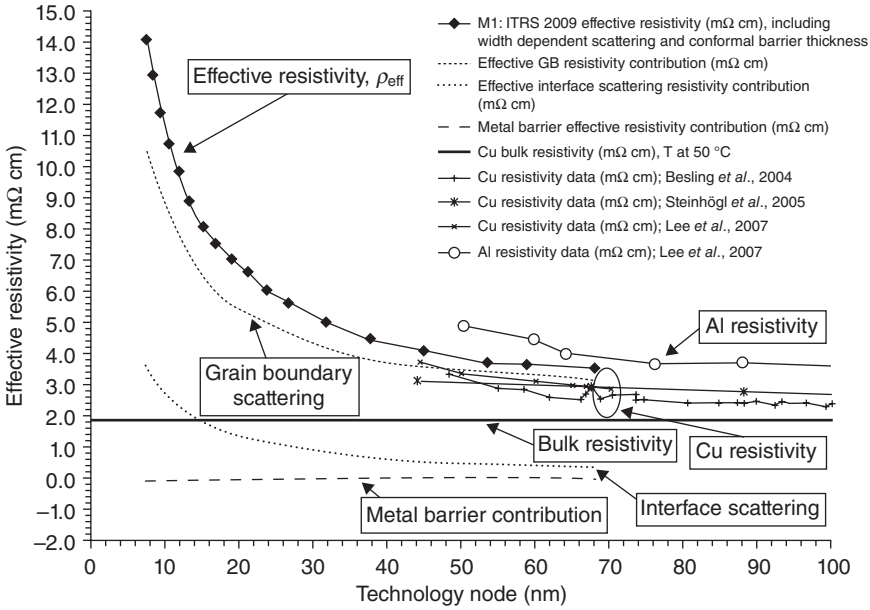


*8.2* Expected interconnect resistivity as a function of technology node (based on metal half-pitch dimension), showing expected trending contributions from different components of resistivity increase. For the model used [Steinhögl *et al.* (2002, 2004, 2005)], grain boundary scattering is dominant. The redundant path provided by the metal barrier does not add to the effective resistivity. The representative Cu resistivity data (Besling *et al.*, 2004; Steinhögl *et al.*, 2005; Lee *et al.*, 2007) shown agrees well with the model trending down to presently accessible metal line widths. Al resistivity data (Lee *et al.*, 2007), shown for reference, lie above the trend graphs found for Cu. The presence of a high resistivity liner that is not easily scaled does not provide a strong argument for Al replacing Cu should increase in the Cu resistivity become intolerable.

ductor with surface scattering. The approximation accuracy compared with the exact integral relationship is estimated by Steinhögl *et al.* (2005) to be better than 3.5% for linewidths between 50 and 1000 nm. The first term in equation [8.1] corresponds with the grain boundary scattering contribution and the second with interface scattering. The values of the other parameters are taken directly from Im (2005) with the exception of the bulk resistivity, where $\rho_0 = 1.85\ \mu\Omega$cm at ~50 °C (348 K) is assumed: $\lambda = 37.3$ nm (300 K), $p = 0.41$, and $R = 0.22$. Similar plots are found in the studies previously noted, and data from those align well with those shown in Fig. 8.2. The parameters $w$ and $AR$ are necessary geometrical parameters that are determined by the ITRS roadmap, and the trending curve for effective resistivity in Fig. 8.2 is directly tied to ITRS predictions from 2007 and 2009. Using

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these parameters, the grain boundary contribution seems larger than that from interface scattering, but surface scattering is argued as being as least as important by others (Gignac, 2007; Graham *et al.*, 2008) in Cu interconnect microstructures where the mean grain size exceeds the electron mean free path. It is likely that there will be improvements in process and integration to improve on the grain structure, size and interface smoothness, but such improvements will not be easily achieved. In fact, the evidence appears to indicate that microstructure development (Brandstetter *et al.*, 2010) and interface quality because of line edge roughness (LER) (Noguchi, 2005) are less easily controlled or perhaps more complicated to address when the line width is decreased. An LER contribution that does not improve with scaling would significantly worsen the resistivity trend (Lopez *et al.*, 2009). Thus, interconnect microstructure that becomes progressively more difficult to control as trench width narrows, adds further complexity to the expected Cu resistivity increase as interconnect critical dimensions scale downwards (ITRS, 2009) in width and thickness.

The result in Fig. 8.2 demonstrates the dramatic resistivity increase expected beyond the 32 nm node, although the accuracy of the prediction needs verification because the result is based on an integral approximation. The published data obtained so far for technologically relevant Cu interconnect does not yet extend down below 40 nm so that the worst of the projected resistivity increase has yet to be verified. Interestingly, resistivity trending for Al interconnect (from Lee *et al.*, 2007) is also shown for reference, and it is clear that Al metallization remains an inferior option down to 50 nm and probably beyond. The reason is that present Al interconnect technology requires the use of TiN antireflective coating (ARC) and a high resistivity Ti/TiN redundant metal liner to mitigate Al susceptibility to stress-induced voids (Okabayashi, 1993; Walls, 1997) or EM (Gambino, 2008; Murphy *et al.*, 2008), and it will be difficult to thin the liners with technology scaling (Rosenberg *et al.*, 2000).

The contributions for grain boundary, interface scattering and the barrier metal are also shown in Fig. 8.2. The barrier contribution shows as a negative because it provides an additional current pathway, which reduces effective resistivity by a very minor amount. This barrier contribution analysis can be seen by treating the interconnect as stemming from two parallel pathways owing to the Cu metal and the metal barrier. The total resistance can be shown to have a form where the barrier metal contribution can be expanded out as $(1 + x)^{-1} \cong 1 - x + x^2$, where $x$ is a term consisting of metal barrier resistivity and cross-sectional area contributions. Note that the above analysis completely ignores vias, which necessarily have barrier metal at the bottom, so that it will have a serial, in addition to the already present parallel, contribution to the via resistance or effective via resistivity. This serial contribution is a seriously detrimental contributor to via resistance

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and can only be scaled downwards by thinning the barrier. This scaling impact of via resistance is presently not a well-addressed or well-documented problem. How via bottom barrier thickness is addressed will potentially have impact on the use of the Short Length Effect (Blech, 1976, 1997, 1998; Filippi *et al.*, 1995; Wang and Filippi, 2001; Christiansen *et al.*, 2008; Oates and Lin, 2008, 2009) for current density enhancement in short-length interconnects because the via bottom barrier serves both as the flux blocking barrier from one lower level interconnect to an upper level interconnect and as the thin membrane to support back-stress development in sufficiently short-length interconnects (Aubel *et al.*, 2007).

According to Meindl *et al.* (2002), interconnect signal latency can be generically expressed as a product of three factors:

$$\tau = (\rho\varepsilon)\left(\frac{1}{ht}\right)(l^2) \qquad [8.2]$$

where $\tau$ is latency of a single isolated interconnect, $\rho\varepsilon$ is the resistivity–permittivity factor, $h$ is the metal height, $t$ is the dielectric thickness, and $l$ is the interconnect length. As technology scales, assuming the rather ideal situation that no additional chip functions are added with scaling, all the physical dimensions in the BeoL stack shrink proportionately so that the only simple way to decrease latency is to improve the properties of the materials used in interconnects; namely, by reducing either the metal resistivity $\rho$, or the effective dielectric permittivity $\varepsilon$. From the metallization perspective, Cu is as good a conductor as can be expected, for a presently available technology. Although improved metallization alternatives to Cu are being investigated (e.g., metal silicides, nano-Ag, carbon nanotubes, nano-graphene, phonon engineering, on-chip optical interconnects, and positive quantum confinement effects; ITRS, 2009), there is little clarity on which technology or technologies will be an appropriate future interconnect medium from a performance, reliability, and manufacturability standpoint; however, the increasing resistivity of Cu metallization as interconnect dimensions scale downwards means that such improvements are critical. Otherwise, the dimensional scaling benefit will be easily lost.

Unfortunately, no new and realistic materials solution presently exists to fully eliminate this upwards resistivity trend of Cu metallization. At this stage, the main effort is to improve on the effective dielectric constant by substituting materials with progressively lower dielectric constant $k$, where $\varepsilon = k\varepsilon_0$ and $\varepsilon_0$ is the permittivity of free space. It is clear, however, that any materials improvement through the use of an ultra low-$k$ dielectric ($k \leq 2.5$) is limited by the presence of higher $k$ etch stop layers ($4.0 < k < 6$) in the present BeoL stack. Significant process optimization effort is required to integrate new materials into a given integration scheme and, although the transition to much lower $k$ materials is a priority for future scaling, such

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effort may come at the possible cost of decreasing the process margin. For BeoL technology at 22 nm and beyond, use of air-gap technology between the interconnect metal and the use of an ultra-thin metal barrier will be necessary to achieve the required performance improvements (Chen *et al.*, 2008). For metal 1 and intermediate layers, the increased BeoL interconnect delay for a fixed length is likely to be very significant by the end of this decade, and, although capacitance is considered to be more important at these levels than resistance, this resistivity trending may not be easily countered by simple chip shrinkage (See Meindl's equation [8.2]) as is presently done. Interconnect delay issues are also a major concern for global (across chip) interconnect wiring because their length does not scale as easily as lower level metal interconnects, but because their lateral dimensions remain large relative to the electron mean free path, they still benefit from the incorporation of ultra low-*k* solutions. Moreover, increased functionality for a given device with technology scaling (so-called system-on-chip or SOC integration) inevitably keeps the overall total wiring length from decreasing as fast from technology node to technology node. Generally, interconnect delay issues can be expected to progressively worsen with each generation and are not easily addressed by new materials substitution in the BeoL, although it might be expected that better process control over the Cu microstructure and interface quality will be forthcoming and that it will provide additional relief from resistivity scaling. By that time, three-dimensional (3D) integration (die stacking and chip-to-chip connection through the Si die) will probably be a stronger technology driving force. In a sense, these latest pre-15 nm Cu-based interconnect technology advances could spell the 'last hey-day' for advanced Cu-based interconnect technology development.

## 8.2 Electromigration (EM) scaling by generation

One of the major reliability benefits that occurred as a consequence of the transition from Al(Cu)-based to Cu-based interconnects was greatly improved EM performance. Such improvement is desired because the trend towards smaller dimensions means that the applied current density increases progressively with each succeeding generation. Beyond a certain point, the increased current density requirements render the use of Al interconnects impractical, except at maybe the highest metal level, where the routing between bond pads is permitted. EM improvement in Cu over Al is naively predictable in that Cu has a significantly higher melting temperature ($T_m$) than Al (1090 versus 660 °C). Thus, for a given temperature, stress on the metal that can lead to metal atom movement would seem less of a problem for Cu than for Al. As an example of the relative difference in EM performance between Al and Cu, work by Hu *et al.* (1999b) demonstrates a

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roughly 100 times improvement in EM performance by Cu interconnect over Al at EM stress conditions.

The actual details about Cu versus Al EM are a bit more complicated owing to differences in how Al interconnects are processed compared with Cu. Al interconnects are created by subtractive etch of the metal film after patterning so that the metal microstructure tends to form grain boundaries that are orthogonal to the substrate plane. Al metal film is doped with a small amount of Cu (ranging from 0.5 to 3 at. wt. %) for improved EM performance by 'grain boundary stuffing' (Hu *et al.*, 1992; Spolenak *et al.*, 1999) and is usually sandwiched between thin layers of Ti below and Ti/TiN above the Al film (Hu *et al.*, 1995). These layers form a so-called redundant shunting layer so that any significant voiding that develops in Al metallization by either EM or SM can be mitigated to a certain degree. The more conventional Al-based interconnects are also terminated by via plugs made of tungsten (W) material to connect overlapping interconnects between adjacent layers. From an EM perspective then, the final flux divergence occurs where the Al interconnect and W plug connect. The Al grains tend to grow vertically from the Si substrate and show preferential (111) orientation, and because the deposition temperature is normally relatively high (≥350 °C), the as-deposited grain size is rather large (≥1 μm). Thus, the as-deposited grains are more or less columnar in nature owing to the relatively high deposition temperature (compared with $T_{m,Al}$). Furthermore, Al benefits from having a naturally forming native and self-limiting surface oxide that creates a very clean and strong interface between metal and oxide layer. This layer tends to limit but not block, any tendency for atomic movement through its surface interface under EM stress. Such a stable interface layer means that the 'fastest pathway' for EM damage is likely to be found through the grain boundaries in several micrometers wide Al interconnects, where polygranularity is more likely (Cho and Thompson, 1989; Walton, 1992). The doping effect from Cu is also important. Research indicates that the Cu dopant depletion from the interconnect cathode end is necessary to initiate EM voiding from grain boundary pathways (Hu *et al.*, 1991, 1992 and 1995). Only after Cu dopant depletion through Al interfaces has extended beyond the EM critical length (Blech, 1976), is grain boundary EM possible. This effect yields a latency effect in observed relative resistance increase during EM stressing. During EM stress, voids can grow across an interconnect line owing to grain boundary diffusion at some point so that resistance increase may be significant enough to be considered an interconnect failure (Sanchez and Morris, 1991), but eventually such voids tend to migrate towards the cathode end where the Al interconnect and W plug meet (Kawasaki and Hu, 1993).

As the Al(Cu) interconnect feature dimension is shrunk toward 250 nm (Hu *et al.*, 1995), grains are found to be generally longer (in the direction

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of the interconnect length) than wide (the width being defined by the metal patterning) for basically the same Al film microstructure so that the Al interconnect grain structure outwardly resembles 'bamboo' shoots lying down on the silicon wafer. Bamboo grain boundaries tend to lie orthogonal to the interconnect length direction. In bamboo-grained, narrow interconnects (~ 250 nm width) grain boundary pathway EM is constrained by the grain boundary orientation, which is orthogonal to the electron flow (interconnect length) direction, and may be the primary geometrical reason for EM performance enhancement (Oates, 1997). In this instance, both interfacial and grain boundary EM mutually contribute to interconnect EM damage, but interface EM is considered dominant (Hu *et al.*, 1995). Finally, Al interconnects are not an extinct species in advanced technology because they are used as a top metal routing layer, especially for 'mixed signal' devices that combine both analog and digital functions (Hein, 2008). Given the discussion above, it is clear that lessons learned about Al interconnect reliability cannot be forgotten and are actually very relevant to the approaches taken to improve EM in Cu nanoscale interconnects.

For Cu, however, use of a damascene integration scheme means that the metal microstructure is formed within the boundaries of the trench features rather than having the interconnect features defined upon an already existing metal film as is the case for Al interconnects. The Cu is deposited using electroplating at relatively low temperature (compared with $T_{m,Cu}$). The Cu microstructure is thus unstable and can be greatly affected by a subsequent thermal anneal or even by just simply leaving the Cu film with overburden intact at room temperature for extended periods (Lingk and Gross, 1998; Harper *et al.*, 1999; Detavernier *et al.*, 2003). The Cu microstructure evolution is three-dimensional with interface boundaries at the trench bottom and sidewalls affecting microstructure evolution. Thus, final grain structure is less bamboo in character, even for the narrowest line widths. The resulting Cu microstructure and texture are thus more variable, although the primary grain orientation may still be more (111) than not. The smaller Cu grain size for very narrow interconnects also has a significant bearing on EM reliability as will be shown later. It is also notable that the Ta-based diffusion barrier along the Cu trench bottom and sidewalls are quite thin and getting necessarily thinner with each technology generation, although possessing a much higher intrinsic electrical resistivity compared with Cu. Thus, this metal barrier liner does not function particularly well as a redundant shunting layer in comparison with the role played by the Ti/TiN in the older Al(Cu) interconnect technology, although its presence does provide the additional benefit of avoiding EM failure by sudden open-circuit (Li *et al.*, 2003 and 2005; Yang, 2005).

Another interesting characteristic of Cu metallization as opposed to Al is that Cu does not possess a stable native oxide like Al does. So, unless the

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Cu surface is well-passivated, this Cu interface is prone to diffusion-controlled damage such as can happen during EM and stress migration (Hartfield *et al.*, 2004). It is then reasonable to suggest that EM in Cu interconnects is generally driven mostly by interface diffusion along a particularly weak interface (Hartfield *et al.*, 2004; Hu *et al.*, 1999a; Lin *et al.*, 2004; Lloyd and Clement, 1995; Michael *et al.*, 2003a; Usui *et al.*, 2004; Vairagar *et al.*, 2004a). Other pathways such as grain boundary diffusion, may also be significant contributors for a given microstructure (Gan *et al.*, 2004 and 2005; Huang *et al.*, 2005; Sukharev *et al.*, 2009; Zschech *et al.*, 2009), especially when linewidth impact on microstructure development becomes important. Presumably, the quality of the interface between the Cu surface and the capping dielectric is controlled mainly by the exposure environment before capping deposition (Birringer *et al.*, 2009). This intuitively reasonable assessment about the EM interface pathway was confirmed by results showing a very strong correlation between interfacial adhesion strength, between a given passivation material and a Cu surface, and EM activation energy (Lane *et al.*, 2003; Lloyd *et al.*, 2005). In this instance, the weakest interface is observed to lie at the trench top, and a primary focus of improving EM reliability has been in developing interface engineering methods to reduce the EM drift velocity at the trench top. In 8.3, process integration approaches that strive to improve the EM performance of known weak interface pathways are described.

Any basic discussion of EM usually starts with the EM drift equation and is expressed as follows:

$$v_{\mathrm{D}} = \frac{J_{\mathrm{F}}}{C} = -\left(\frac{D_{\mathrm{eff}}}{k_{\mathrm{B}}T}\right)\left[Z^{*}_{\mathrm{eff}} \cdot eE - \Omega\left(\frac{\partial \sigma}{\partial x}\right)\right] \qquad [8.3]$$

where $v_{\mathrm{D}}$ is the atomic drift velocity, $J_{\mathrm{F}}$ is the atomic flux, $C$ is the local atomic concentration, $D_{\mathrm{eff}}$ is the effective diffusivity, $k_{\mathrm{B}}$ is Boltzman's constant, $T$ is the temperature, $Z^{*}_{\mathrm{eff}}e$ is the effective charge, $E$ (= $\rho j$, where $\rho$ is the electrical resistivity and $j$ is the electrical current density) is the electric field strength, $\Omega$ is the atomic volume, and $\partial\sigma/\partial x$ is the stress gradient along the interconnect length (which leads to the Blech or short-length effect). The above equation is derived from the Nernst–Einstein relation. Note that the $E = \rho j$ factor captures nicely the impact of scaling on EM. As interconnects scale dimensionally, both $j$ and $\rho$ necessarily increase. The current density $j$ increases because the interconnect cross-sectional area shrinks by about two-fold each generation and because the sustaining transistor drive currents probably increase. The Cu resistivity $\rho$ increases because increasing contributions by grain boundary and interface scattering are found as interconnects narrow (Besling *et al.*, 2004; Rossnagel and Kuan, 2004; Zhang *et al.*, 2004a, 2004b; Steinhögl *et al.*, 2002, 2004, 2005; Tay *et al.*, 2005; Shimada *et al.*, 2006; Yarimbiyik *et al.*, 2006). Other potentially important

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chemical potential gradient terms such as the Soret effect (temperature gradient) and entropy gradient (Lloyd, 1999; Croes *et al.*, 2010) should be taken into account but for brevity they are not covered in this chapter. Hu *et al.* (1999a) have previously demonstrated how EM lifetime and interconnect scaling track with one another. The interconnect lifetime is estimated typically using the venerable Black's Equation (Black, 1967; 1969), which is given as

$$t_{\text{Fail}} = Aj^{-\text{n}} \exp\left(\frac{\Delta H}{k_{\text{B}}T}\right) \qquad [8.4]$$

where $t_{\text{F}}$ is the average time to fail, $A$ is a constant, $j$ is the current density, $n$ is the current exponent, $\Delta H$ is the activation enthalpy, $k_{\text{B}}$ is Boltzman's constant, and $T$ is the absolute temperature. The value of $n$ should range between 1 and 2, where $n = 1$ represents void-growth-limited failure and $n = 2$ represents void-nucleation-limited failure. Equation [8.4] above is used to characterize the generic behavior of the interconnect population, and statistical analysis is necessary to fully characterize the entire population of interconnects within a microelectronics device. Cu interconnect EM tends to preferentially exhibit void-growth limited behavior with $n$ ranging experimentally between 1 and 1.4 (Hau-Riege *et al.*, 2003; Hau-Riege, 2004; Lloyd, 2007). Current exponent values >1 indicate that a fraction of the interconnect population is void-growth limited although the remaining fraction is void nucleation limited. Note that when $1 < n < 2$, Equation 8.4 tends to lose its physical meaning somewhat, although it is rather convenient to use it regardless. Bear in mind, however, where $n$ does not equal 1 or 2 exactly, Black's equation should be used with some care (Lloyd, 2007).

Using the drift velocity equation [8.3], the characteristic lifetime, $\tau_{\text{D}}$, is written as

$$\tau_{\text{D}} = \frac{\Delta L_0}{v_{\text{D}}} = \Delta L_0 \left(\frac{hk_{\text{B}}T}{\delta_{\text{i}} D_{\text{i}} F_{\text{i}}}\right) \qquad [8.5]$$

where $\Delta L_0$ is the critical void size for interconnect failure and is demonstrated by Fig. 8.3a. The other parameters are the thickness $h$, temperature $T$, interface pathway thickness $\delta_{\text{i}}$, pathway diffusivity $D_{\text{i}}$, and the interface EM driving force $F_{\text{i}}$. In Fig. 8.3b, the corresponding points in the resistance trace for when a critical void size $\Delta L_0$ is reached and where additional material drift to an extent $\Delta L_{\text{d}}$ occurs are shown. This parameter $\Delta L_0$ scales with the via size for a given technology node (e.g. 130 to 90 to 65 to 45 to 32 to 22 nm). The via size decreases roughly by about 70% per side, per technology transition, although the maximum current density $j_{\text{max}}$ is projected to scale upwards by roughly 30% per generation (ITRS, 2009; Iwai, 2009). The characteristic lifetime would then be expected to decrease

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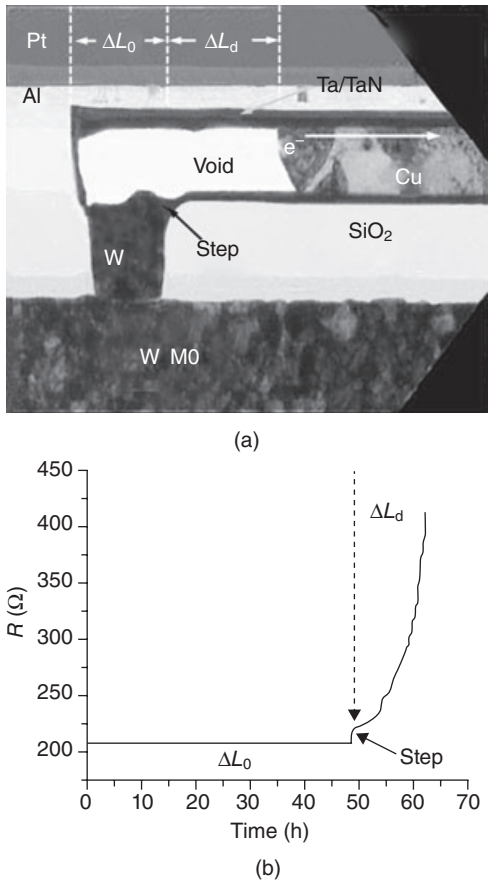


*8.3* (a) Void formation at the cathode end must reach a certain size to generate interconnect failure. This critical volume is conveniently defined by a length parameter $\Delta L_0$, which is roughly the size of the contact via. This critical size scales downwards with the technology node and is essentially one of the root factors in the decrease in EM lifetime with technology node. Additional material depletion, represented by $\Delta L_d$, generates gradual resistance increase by the so-called material 'drift.' (b) The change in resistance overtime shows resistance features that correspond to $\Delta L_0$ and $\Delta L_d$ [from Hu *et al.*, 2004 (© 2004 IEEE); permission IEEE; images have been digitally enhanced from the original for publication purposes].

0.7/1.3 ~ 0.5 per technology generation (Hu *et al.*, 1999a) or a nearly 10-fold decrease in EM performance within three generations! This critical void size-constrained trending of EM lifetime is demonstrated by the plot in Fig. 8.4 for single damascene W plug terminated lines from Hu *et al.* (2004). Yokogawa and Tsuchiya (2004) showed a line width dependence of EM

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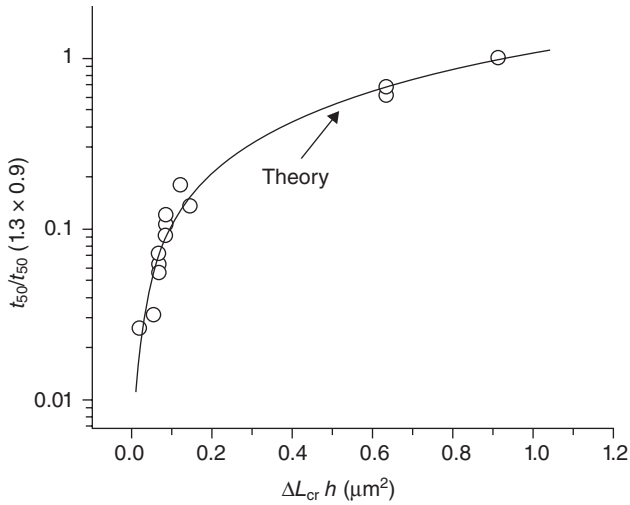


*8.4* Relative impact of critical void volume on EM lifetime (From Hu *et al.,* 2004 (© 2004 IEEE); permission IEEE).

lifetime following a power law behavior ($t_{50} = Aw^N$) with exponent $N \sim 1.8$ using standard Kawasaki–Hu test structures; however, the picture of a decreasing EM margin remains unchanged. Hence, the substantial EM margin originally afforded by a transition to Cu-based interconnects will have been seriously eroded for pending technology generations unless new integration or process strategies are implemented to restore the EM performance margin.

Equation [8.3] strictly applies before complicated void nucleation and growth events occur, but it can be used to illustrate that EM in Cu interconnects is happening across several separate pathways (Hau-Riege, 2004; Hu *et al.*, 1995 and 1999a; Li *et al.*, 2004; Ogawa *et al.*, 2002; Yokogawa, 2008). A depiction of these pathways is shown in Fig. 8.5. At the expense of some complexity, a somewhat different representation of the pathway dependences from those shown in the other studies is used for further discussion:

$$\begin{aligned} Z^*_{\text{eff}} D_{\text{eff}} &= Z^*_{\text{b}} f_{\text{b}} D_{\text{b}} + Z^*_{\text{p}} \rho_{\text{disl}} a_{\text{core}} D_{\text{p}} \\ &+ Z^*_{\text{gb}} \sum\nolimits_k \delta_{\text{gb;k}} D_{\text{gb;k}} \left\{ \frac{[\text{TRUNC}(w/d_{\text{W}}) - 1]}{(d_{\text{W}} |\cos\varphi_{\text{gb}}|)} \right. \\ &\left. + \frac{[\text{TRUNC}(h/d_{\text{H}}) - 1]}{(d_{\text{H}} |\cos\psi_{\text{gb}}|)} + \frac{1}{(d_{\text{L}} |\tan\theta_{\text{gb}}|)} \right\} \\ &+ Z^*_{\text{mbi}} D_{\text{mbi}} \left[ \delta_{\text{mbi}} \left( \frac{1}{w} + \frac{2}{h} \right) \right] + Z^*_{\text{cbi}} D_{\text{cbi}} \left( \frac{\delta_{\text{cbi}}}{w} \right) \end{aligned} \quad [8.6]$$

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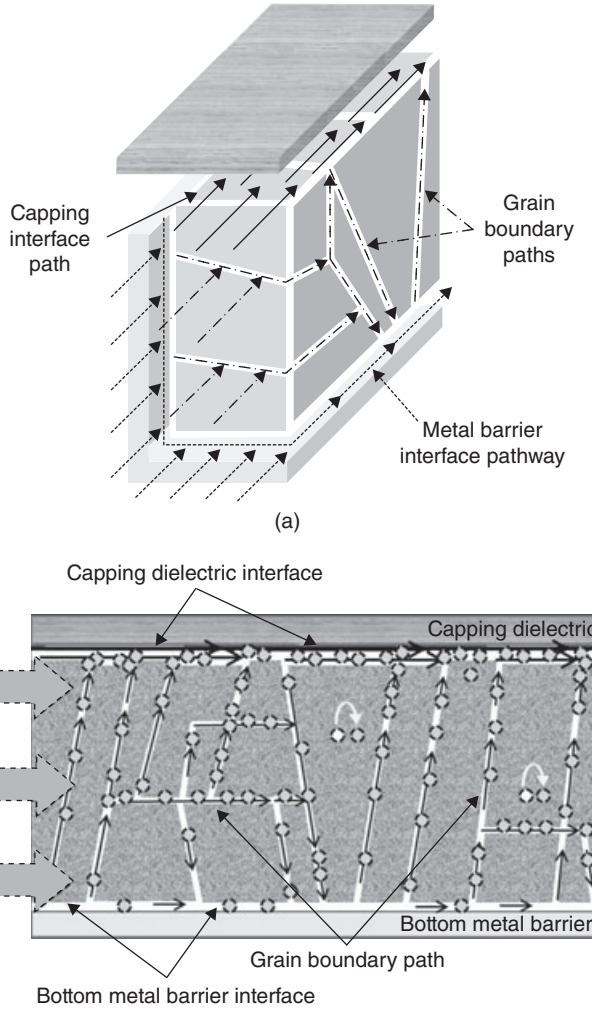


*8.5* (a) Exploded view of major EM pathways; for simplicity, bulk and pipe EM pathways are not shown. (b) Cross-sectional view of EM pathways showing the multiple possibilities for mass transport within a given microvolume. Within such a microvolume, various pathways connect to enable mass transport over larger distances. Grain boundaries are inherently unable to transport mass of over distances if they do not form a continuous mass transport pathway along the entire interconnect length. Interfaces, however, run along the entire interconnect length to enable long-distance mass transport of EM-driven atoms. Thus, interfaces do not need to be the fastest mass EM pathway locally, only globally, and it is the fastest of the interface pathways that acts as the 'rate-limiting path' for long-distance EM mass transport. Such multiple pathway connections intuitively indicate that localized flux divergences where pathways with different mass transport capabilities may meet are a natural consequence of the multi-pathway model.

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where $D_{eff}$ is the effective EM diffusivity and $D_A$ are the respective diffusivities for each pathway ($A \equiv b$, *gb*, *mbi*, *cbi*, and *p* for bulk, grain boundary, metal barrier interface, capping barrier interface, and pipe diffusion pathways, respectively). $Z^*_{eff}$ is the effective charge parameter, and the parameters $Z^*_B$ are the effective charges for the different EM pathways ($B \equiv b$, *gb*, *mbi*, *cbi*, and *p* for bulk, grain boundary, metal barrier interface, capping barrier interface, and pipe diffusion pathways, respectively). The other parameters are $f_b$ (fraction of atoms in the bulk), *w* (line width), *h* (line height), $d_C$ [average grain size in the $C \equiv w$ (width), *l* (length) and *h* (height) directions, respectively], $\rho_{disl}$ (dislocation density), $a_{core}$ (dislocation core cross-sectional area), and $\delta_D$ (pathway width, $D \equiv gb$, *mbi*, and *cbi* for grain boundary, metal barrier interface, and capping barrier interface pathways, respectively). For clarity, $\delta_{gb;k}$ is the grain boundary width of the *kth* grain boundary within a given pathway volume and not the identity matrix element, $\delta_{ij}$. The EM path is assumed to cover a given volume, such as $V_{path} = lhw$, so that the grain boundary and dislocation sums account for all grain boundary and pipe diffusion pathways, respectively, within that volume. This pathway model is illustrated in Fig. 8.6. It is convenient to partition the sum for grain boundary EM as a sum within an average grain length $d_L$. In Fig. 8.6a, such a boundary volume is shown that contains a single width spanning grain boundary with angle $\theta_{gb}$. There are three grain boundary terms to cover grain boundaries that lie parallel, or nearly parallel, to the interconnect length, width or height. The factor $\tan\theta_{gb}$ defines the average grain boundary angle for a grain boundary spanning along the interconnect height and width relative to the surface normal from the trench bottom ($0 < \theta_{gb} < 180°$). The angle $\varphi_{gb}$ defines the average grain boundary angle for one lying along the interconnect height and length, where $\varphi_{gb} = 0$ means that such a grain boundary is parallel to the interconnect sidewall. The angle $\psi_{gb}$ defines the grain boundary angle for one lying along the interconnect width and length. Likewise, $\psi_{gb} = 0$ means that such a grain boundary is parallel to the interconnect trench bottom. For simplicity, one assumes that both $\varphi_{gb}$ and $\psi_{gb}$ are ~0°. The truncation function, 'TRUNC()' calculates the average number of grain boundaries that lie within the grain length $d_L$ for a given grain orientation (Excel, 2007). For example, if $2 \leq w/d_W < 3$ for grain boundaries along the height (i.e., interconnect trench thickness) direction, then effectively one grain boundary is found along this direction. The $\tan\theta_{gb}$ parameter takes care of the fact that interconnects with grain boundaries spanning the interconnect cross-section and lying parallel to the surface normal ($\theta_{gb} = 90°$) cannot contribute to EM since the current flows along the length direction. Thus, an interconnect with grain boundaries that all have their surface normal vectors pointing parallel with the length direction is a bamboo interconnect; however, the previous statement is an idealization in the sense that a grain boundary path at the point where the

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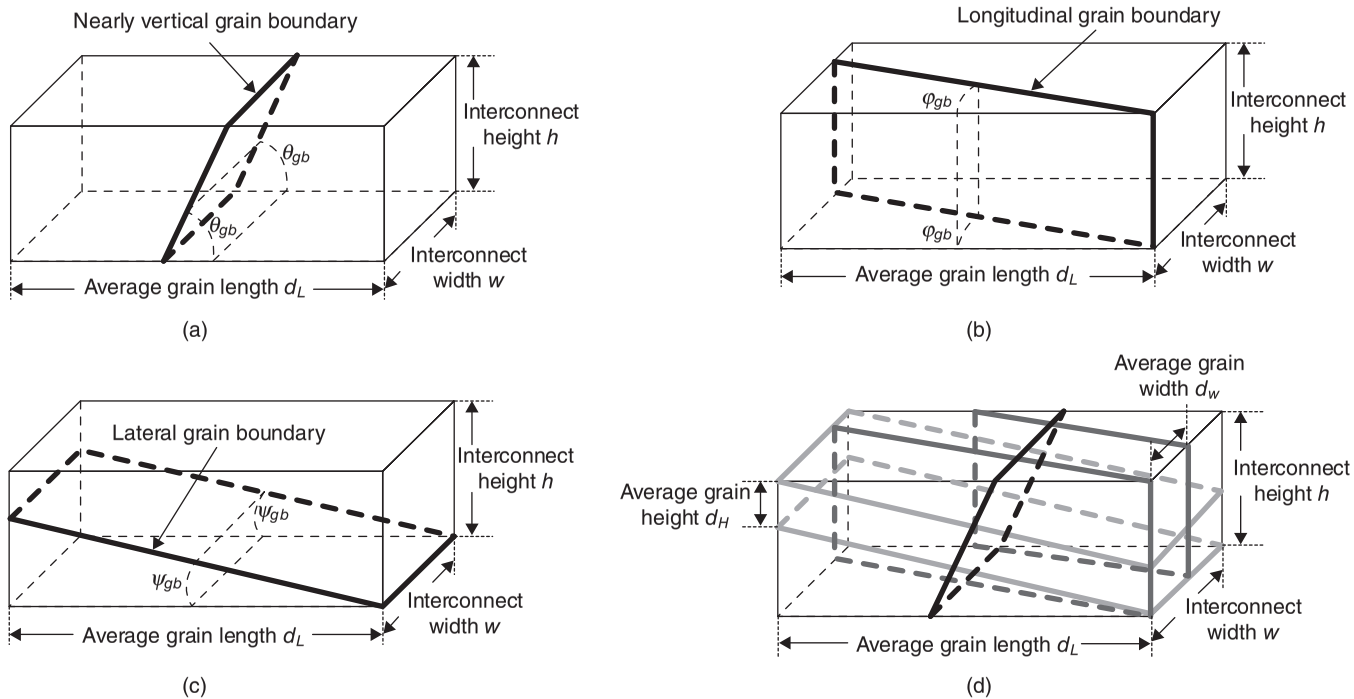
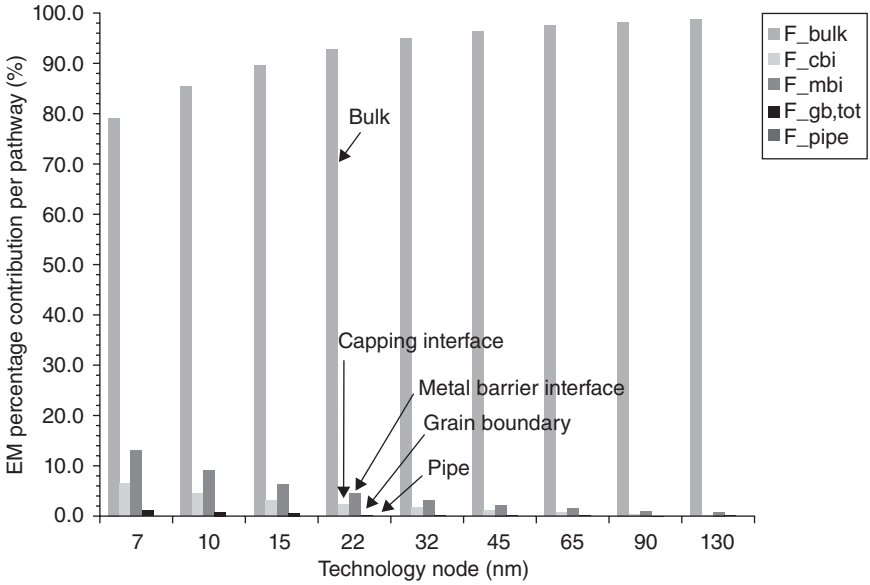
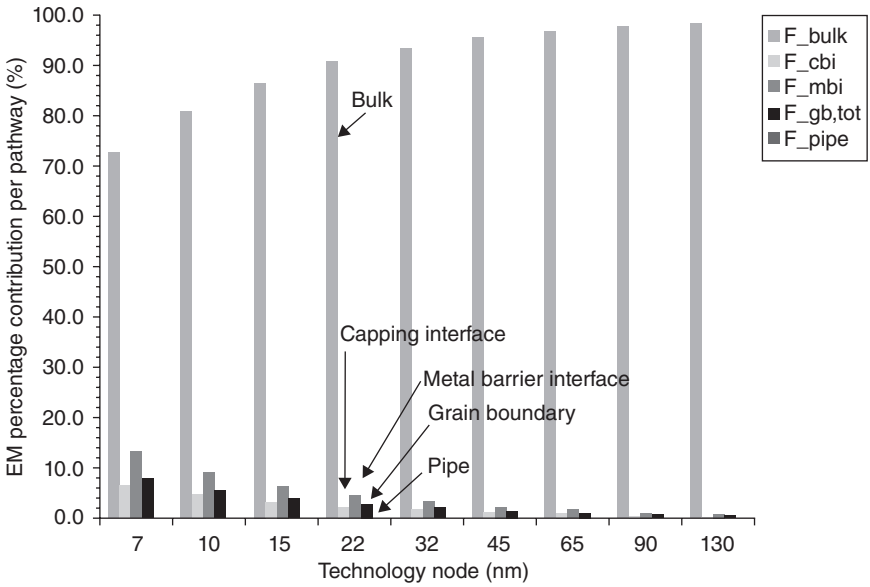



*8.6* Grain boundary angles and averaged grain sizes with interconnect microvolume illustrating the geometrical parameters for the grain boundary pathway calculation: (a) nearly vertical grain boundary; (b) longitudinal grain boundary; (c) lateral grain boundary; and (d) all grain boundaries.




(a)




(b)

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grains terminate at the interfaces is likely to have some rounding so that $\theta_{gb} = 90°$ cannot strictly apply to the grain boundary at that juncture. In that case, a grain boundary triple point exists where a local flux divergence can occur and is a possible site for void nucleation and growth. The factors within each interface transport term that involve a ratio of geometrical parameters such as the pathway width $\delta_C$ to a physical dimension such as line width $w$ or line height $h$ provide a rough estimate of the fraction of atoms involved within a given pathway. A similar statement is made for the product of the dislocation density $\rho_{disl}$ and core area $a_{core}$. For calculations, the effect of grain boundaries on core diffusivity is neglected for simplicity (Budiman *et al.*, 2009).

To get a sense of the relative fractional atomic contributions, it is worthwhile to calculate some EM numbers. To do so, we make some simplifications by breaking up a long interconnect into simple sub-units limited by the average longitudinal grain size $d_L$. We assume that the volume of interest occurs within a grain boundary length, i.e. $l = d_L = 200$ nm, so that the sums are greatly simplified. We also assume that the lateral and vertical grain sizes $d_W$ and $d_H$ respectively, equal the line width $w$ and line height $h$ ('bamboo-ish grains') and that the other interconnect dimensions are $w = 100$ nm and $h = 200$ nm. The dislocation density $\rho_{disl}$ is assumed $\sim 1 \times 10^{-3}$ dislocations nm$^{-2}$ (Budiman, 2007) and $a_{core} = 0.82$ nm$^2$ (Frost and Ashby, 1982a, 1982b). With these values, one finds that 98.34% of the Cu atoms lie within the bulk. Interestingly, only ~0.09% is available for the grain boundary. For the interfaces, the metal barrier interface occupies 1%, whereas the capping dielectric interface uses 0.49% of the atoms. The pipe dislocation fraction is ~0.08%. In Fig. 8.7a and 8.7b, we show how the relative contributions to the EM pathway changes with interconnect dimension, where we compare the relative fractional EM contributions per pathway. Here, we assume that the aspect ratio, $AR = h/w = 2$ throughout and that the

*8.7* Estimated atomic fraction for given EM pathway as a function of technology node: (a) assuming that Cu grains are basically columnar across all technology generations; (b) assuming that Cu grains are somewhat polygranular along the depth of the trench across all technology generations. For both cases, an aspect ratio $AR = h/w$ is assumed to have a fixed value, AR = 2, where $h$ and $w$ are, respectively, the interconnect height and width. The terms *F_x*, where *x* = bulk, cbi, mbi, gb, and pipe, refer, respectively, to bulk/lattice, capping barrier, metal barrier, grain boundary, and pipe diffusion EM pathways. With continued technology scaling, there is an increasing fraction of Cu atoms within an interconnect lying at interfaces. Polygranular interconnects also show increasing pathway contribution from grain boundaries as technology scales below 15 nm.

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longitudinal grain boundary dimension scales as $2w$. We also assume for simplicity the presence of rectangular grains. The average grain boundary angle is arbitrarily assumed to be $\theta_{gb} = 70°$ from the trench bottom plane for grains that span the interconnect cross-section. For grains with boundaries lying roughly parallel to sidewall or trench bottom, we assume that the boundaries are perfectly parallel with the current flow direction. In Fig. 8.7a, only dimensional scaling is assumed. With technology scaling down to 7 nm, we can clearly see the increasing fractional contribution from the interfaces; however, the grain boundary contribution is not significant because the grains are roughly columnar. In Fig. 8.7b, we assume an average of two grains in the vertical direction and average lateral grain size equaling the width. In this instance, the grain boundary fraction continues to increase with technology scaling so that by the 7 nm node, more than nearly 30% of the available atomic volume follows a non-bulk pathway. Much wider leads (>2 μm) have different weighting because a single average grain is unlikely to span the width so that for polycrystalline interconnects, the grain boundary contribution has additional significance (Hu *et al.*, 1999a).

The individual diffusivities have the form $D_{Path} = D_{0,Path}\exp(-\Delta H_{Path}/k_B T)$, where $\Delta H_{Path}$ is the activation enthalpy for a given mass transport pathway. Convenient reference values for the Cu pathway-dependent activation energies can be found in Lloyd's paper (1999): (i) $\Delta H_b = 2.3$ eV for bulk diffusion, (ii) $\Delta H_{gb} = 1.2$ eV for grain boundary diffusion, (iii) $\Delta H_i = 0.7–1.0$ eV for interface diffusion. For surface diffusion, we use the value provided by Jo and Vook (1995), $\Delta H_s \cong 0.5$ eV since EM was done under ultra-high vacuum conditions. Actually determining, for example, the individual $Z^*$ parameters is not simple because of the complication of developing and testing a number of test structure types where the impact of the certain EM pathway contributors are limited, relative to other pathways. Table 8.2 shows some representative values for $\Delta H$, $D_0$, and $Z^*$. The range of value obtained is quite large and shows the inherent difficulty in using these values for quantitative reliability assessment or projection. Both the $Z^*_{Path}$ and $D_{Path}$ values at a given temperature dominate the relative EM contribution. So, simple atomistic bookkeeping does not tell the whole story. To provide a picture of the EM trending as a function of EM pathway, some calculations can be made using values from Tables 8.1 and 8.2. For this calculation, one goes back to equation [8.3], ignoring the back-stress term, and calculates the drift rates for the different pathways. Several assumptions also need to be made. First, representative values from the literature are chosen from Table 8.2. Second, a grain size characteristic is chosen to distinguish between microstructure that is essentially bamboo or columnar and one that has transverse grains whose boundaries lie parallel to the EM current. Third, where values are not found in the literature, a 'guess' value is used that is based on the reported value for somewhat

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*Table 8.2* Pathway dependent Cu electromigration diffusion and kinetic parameters

| Diffusion pathway[a] | Activation enthalpy $\Delta H$ (eV) | $D_0$ ($cm^2 s^{-1}$)[b] | $Z^*$[c] |
|---|---|---|---|
| Bulk or lattice | 2.30 [1]<br>2.04 [2] | 0.2 [2]<br>3.4 [4] | –5.5 to –26 [6]<br>–15 [15] |
| Grain boundary | 1.20 [1]<br>1.08 [2]<br>1.07 [3,11][d]<br>0.75–0.87 [8]<br>0.82 [16] | 0.1 [2]<br>0.22 [3]<br>0.06 [5]<br>$2.32 \times 10^{-2}$ to $7.78 \times 10^{-3}$ [8]<br>$3.35 \times 10^{-2}$ [11][d]<br>$1.55 \times 10^{-2}$ [16] | –14 [5] |
| Metal barrier interface | 0.70 to 1.0 [1]<br>0.70, 1.4 or > 1.8 [7]<br>1.4 [11][d] | 0.11 [11][d]<br>0.22 [13] | –0.8 [14] |
| Capping barrier Interface, $SiC_xN_y$ | 0.70 to 1.0 [1]<br>0.80 to 1.0 [7]<br>0.54 [3][e]<br>0.66 [3][f]<br>0.87 [12] | $1.28 \times 10^{-10}$ [3][e]<br>$2.2 \times 10^{-7}$ [3][f]<br>$4.75 \times 10^{-3}$ [17] | –0.8 [14] |
| Capping barrier interface, $CoW_xP_y$ | 1.8 to 2.0 [9] | $4.8 \times 10^{-3}$ [17] | –0.8 [14] |
| Pipe[c] | 1.2 [2] | $3.2 \times 10^{-5}$ [2]<br>0.06 [11] | –14 [14] |
| Surface | 0.47 [10] | 0.26 [5] | –0.8 [5] |

[a] [1] Lloyd, 1999; [2] Frost and Ashby, 1982a, 1982b; [3] Gan *et al.*, 2005; [4] Chao *et al.*, 2007; [5] Hu *et al.*, 1999; [6] Butrymowicz *et al.*, 1973; [7] Hu *et al.*, 2003, 2010; [8] Surholt and Herzig, 1997; [9] Hu *et al.*, 2004a; [10] Jo and Vook, 1995; [11] Singh *et al.*, 2004; [12] value assumed by author, using [1], and seems good fit overall from literature; [13] value assumed by author, using [3] grain boundary diffusion value; [14] value assumed by author, using [5]; [15] assumed by author, using [6]; [16] value assumed by author, using [8]; [17] value assumed by author, based on comparing published EM data from 130 to 500 nm, where the dielectric capping interface diffusion is still dominant. This value is not necessarily true to CoWP capping; however, I have used it simply for comparison purposes. Underlined values were chosen for calculations to compare relative EM drift velocities. Where possible, parameters such as $D_0$ and $\Delta H$ were matched to the same paper, although it is generally not possible to do so for all parameters at the same time, especially $Z^*$.

[b] For $D_0$ estimate, results are usually quoted as $\delta_{bndry} D_0$, where $\delta_{bndry}$ is the boundary width. To convert to $D_0$, a value of $\delta_{bndry} = 0.5$ nm is assumed. For pipe diffusion, the core cross-section is estimated by assuming that the core radius, $R_0 \sim 2b \sim 0.5$ nm, where $b$ is the Bergers vector value for Cu.

[c] Certain values, such as $Z^*$ for interfaces, have been assumed for calculations described in the text and these generally should not be used as reference values if better values are available. Calculations using such assumed values should be considered with care.

[d] For reference [11], GB $D_0$ is calculated using grain boundary width of 0.5 nm and activation energy of 1.07 eV, consistent with reference [3]. For the metal barrier interface, interface width is assumed to be 0.5 nm and activation energy used is 1.4 eV from reference [7].

[e] From reference [3], $D_0 = 1.28 \times 10^{-10}$ $cm^2 s^{-1}$ goes with activation energy 0.54 eV.

[f] From reference [3], $D_0 = 2.2 \times 10^{-7}$ $cm^2 s^{-1}$ goes with activation energy 0.66 eV.

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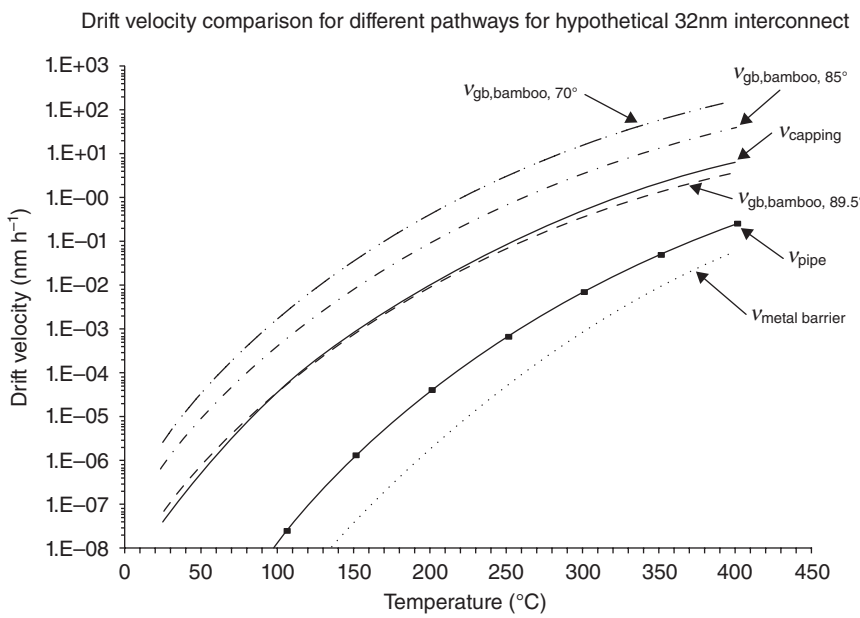
related work (a dangerous assumption but used here to illustrate some points). These simplistic calculations are then assuming that all pathways are continuous from the interconnect cathode to the anode.

By assuming the above, one immediately finds a slight conundrum with regards to the grain boundary drift rate. The drift rate can turn out much higher than would be expected during typical EM testing at high temperature because the $D_0$ values reported (measured by other means) are essentially much higher than that obtained for interface diffusion from 25 to 400 °C (see Fig. 8.8). In Fig. 8.8, the grain boundary pathway only becomes slower than the capping interface pathway when the columnar grain boundary is very close to 90° and actually still outpaces the interface pathway at a higher temperature. From Table 8.2, the grain boundary $D_0$ value can be greater than $1 \times 10^6$ times the value estimated for capping dielectric interface diffusion. One major flaw with the present analysis is that $D_0$ param-




*8.8* Calculated drift velocities for hypothetical 32 nm interconnect using ITRS 2009 values for $j_{max}$ = 2.0 MA cm$^{-2}$ and $\rho_{Cu}$ corrected for pathway but using estimated value at 105 °C. $D_0$, $\Delta H$, and $Z^*$ assumed underlined values from Table 8.2. Drift rate for grain boundary diffusion can outpace that for interface diffusion depending on columnar grain boundary angle. It should be noted here that the drift picture probably changes once the void is generated and the transport pathway involves free surfaces and alters the local grain boundary structure.

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eters are not directly coupled with appropriate $Z^*$ values, which are typically measured together during EM stress and are not easily decoupled without additional characterization; however, it is still instructive to examine where the analysis breaks down. Although the capping barrier and metal barrier interface $D_0$ values are also guessed values, they lead to EM lifetimes (when coupled with appropriate $Z^*$ values in Table 8.2) that appear reasonable at test and use conditions previously reported (when comparing results from different studies). It is natural to ask why reported values for diffusion parameters do not translate directly to EM drift analysis when there should be nothing inherently different about a diffusion process that involves different driving forces such as thermal stress or a chemical potential or EM.

For the simple pathway model to strictly apply, a continuous pathway for grains must exist that is essentially along the interconnect length; i.e., the grains need to be polygranular within the interconnect for the entire length; however, this situation is not likely for interconnects used in advanced technology. There are bound to be certain sections where polygranularity exists, but these regions will be interrupted by regions consisting of bamboo-type grains or very low-diffusivity twin grain boundaries. Thus, the mass transport is inevitably gated by the movement of material from grain boundaries to the interface pathways that extend along the entire interconnect length. Hence, the EM picture for damascene interconnects is not unlike that found for the earlier Al(Cu) technology. When grains become bamboo-like, EM lifetime becomes rate-limited by the interfaces. This argument then requires that certain grain boundaries that form a 90° angle with the trench bottom must completely span the interconnect width and block or at least delay the mass transport; otherwise, a percolative path through the interconnect for grain boundary mass transport exists. Alternatively, the more mundane explanation is that the $Z^*D_0$ values need to be recalibrated and better reconciled with diffusivity values estimated by other methods so that the parameters used for grain boundary transport yield drift rates that are slower than interface diffusion.

However, the risk associated with longitudinal grain boundary pathways should not be ignored, because the occurrence of polygranularity at certain vulnerable locations (under or within vias) leads to less desirable early EM failures. For example, small grains placed under vias can be likely candidates for early EM failure where the void appears more slit-like but along a horizontal plane, and such slit void EM failures may be more prevalent in narrow interconnects where the effect of the Cu overburden has very little impact on the evolving trench microstructure during anneal. In such a case, the overburden-controlled microstructure may only partially penetrate into the damascene trench and leave only a shallow footprint of a Cu grain at the top of the trench after CMP removal of the overburden. Such a shallow

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grain could then lead to horizontal slit voids under EM stress if a via happened to be placed over it during subsequent processing because the critical void volume for interconnect failure is smaller than the expected via area X trench height (see equation [8.5]). In fact, Oates and Lee (2006) have argued that such horizontal slit-voids fundamentally limit EM reliability.

Although equation 12.4 is conceptually important, it is also a simplification in the sense that the pathways are not really independent but rather contribute in parallel and in series simultaneously along the interconnect length. As an example, grain boundary paths inevitably intersect interface paths and vice versa; these are known as 'triple points' at which localized void nucleation is possible and thus alters the local EM pathway environment. For simulations, only the most important contributions to the EM flux are included into the more general mass balance equation that includes contributions from diffusion, EM, thermal migration, and stress migration (Kteyan *et al.*, 2007; Sukharev and Zschech, 2004; Sukharev *et al.*, 2009; Zaporozhets *et al.*, 2005). From the process engineering perspective, equation [8.4] points to potential avenues where improvement efforts should be focused to increase Cu EM reliability.

## 8.3 Suppression by metal capping: blocking rate-limiting EM pathways

The multiple pathways for EM mass transport and the architecture of the Cu dual damascene process provide various means by which Cu interconnects can fail through void generation and growth. From an EM perspective the ultimate flux boundary lies at the bottom of a dual damascene via, which separates lower interconnect from upper. Thus, fatal interconnect voids can be formed above or below the via bottom barrier liner, and these locations are the likely final void location after long-term EM stress. Whether the void forms above or below the via bottom depends, of course, on the electron flow direction so that the terms 'up-' and 'down-direction' (Ogawa *et al.*, 2002) or 'via-' and 'line-depletion' (Li *et al.*, 2004)) EM have been used to distinguish the two major EM damage modes. Furthermore, different critical void failure locations during up-direction EM stress have led to bi-modal lifetime behavior. Critically large enough voids can form either within the via or the trench so that two lifetime distributions may be evident (Ogawa *et al.*, 2001) and depend upon whether small defects are present within the via that lead to premature EM failure within the via or not (Kim and Wong, 2003). When comparing EM lifetimes for down- versus up-direction, lifetimes are typically shorter for the down-direction because the necessary critical void size is apparently smaller for voids under a via than for voids forming within a via or trench during up-direction EM

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stressing (Gan *et al.*, 2001; Lee and Oates, 2006). If the voiding is severe enough within the trench, failure can also occur when the void size has increased enough to span the interconnect trench (Meyer and Zschech, 2007; Sukarev and Zschech, 2004; Sukarev *et al.*, 2009; Zschech *et al.*, 2009).

From a scaling perspective, certain trends continue to lower the EM advantage found generally in Cu interconnects. Firstly, the pathway model shows that, as the interconnect cross-section is generically decreased, the interface EM contribution increases because the relative fraction of atoms within a given pathway increases as the interconnect dimensions decrease when compared with the bulk fraction $n_b$. For example, for the capping dielectric pathway, the atomic fraction scales as $\delta_{cdi}/h$. A smaller required critical volume for interconnect failure along with an increased contribution to voiding at the trench top interface is thus not an ideal situation. Secondly, although the metal barrier thickness is projected to thin proportionately with interconnect dimension, the ability to thin the barrier depends strongly on its effectiveness in preventing Cu from entering into the adjacent low-*k* dielectric; otherwise, a catastrophic interconnect failure owing to Cu metal shorting between adjacent interconnects results. Because the relative amount of current flowing through the barrier metal compared with the Cu is proportional to the ratio of the resistivity of Cu to the barrier metal (say 4 μΩ cm versus 200 μΩ cm), only about 2% of the current would be expected to pass through the barrier metal. Thus, unless the barrier thickness is reduced to keep pace with technology needs appropriately, the current density burden becomes progressively worse than might be expected from simple dimensional scaling. Another concern about a progressively thinning barrier with scaling might be the resulting Cu microstructure because Cu seed quality is affected by barrier quality. Thirdly, the inevitably increased current density that results from interconnect dimensional scaling (and increasing transistor drive current requirements) and ultra low-*k* dielectrics possessing very poor thermal conduction properties lead to significant increases in the Joule heating burden. Thus, the need to develop improved EM reliability performance is critical for additional technological progress.

Because of the critical role played by the interfaces in EM, interface engineering at the trench top has been a primary area of research focus to improve the EM margin. Such interface engineering effort has led to novel solutions to improve EM reliability. Studies have compared several different types of trench capping metallization, such as $CoW_xP_y$, $CoSn_xP_y$, $CoW_xB_yP_z$, Pd, $Ta/TaN_x$ (physical vapor deposition or PVD), W and Ru (Almog *et al.*, 2007; Hu *et al.*, 2002, 2003, 2004, 2008; Saito *et al.*, 2004; Yang *et al.*, 2009). The general method for such a metal cladding uses selective electroless deposition (Petrov *et al.*, 2002). Selective electroless deposition

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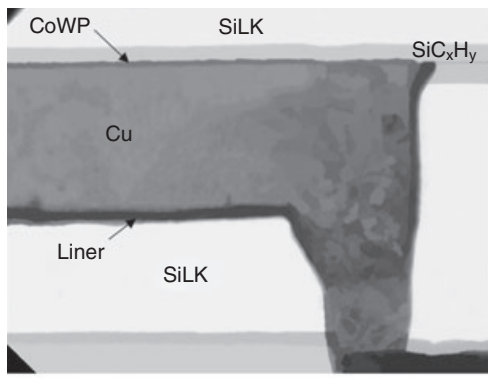
(SED) is a process where autocatalytic or chemical reduction of aqueous metal ions in conjunction with anodic oxidation of a reducing agent takes place on a metal surface without application of an electrical current. SED is attractive from a processing perspective for several reasons. It has generally low process temperature, high surface deposition selectivity, and good self-alignment properties. The metal cladding selectively coats itself on top of the Cu trench after Cu metallization has undergone CMP and does not generally deposit itself onto exposed dielectric lying between any Cu trenches. In Fig. 8.9, an interconnect with a $CoW_xP_y$ capping layer on top of a Cu trench is shown.

The $CoW_xP_y$ was initially suggested as a corrosion and diffusion barrier as well as a potential redundant metal liner (Shacham-Diamand *et al.*, 1999; Kohn *et al.*, 2001; Petrov *et al.*, 2002) because of its relatively low resistivity of 80 μΩ cm. $CoW_xP_y$ diffusion barrier properties have been demonstrated at ~100 nm thickness and as low as 30 nm with a higher temperature anneal. W and P atomic placement into the Co grain boundaries is apparently necessary for good barrier performance (Kohn *et al.*, 2001). Subsequently, Hu *et al.* (2002) showed that very substantial gains in EM performance can be obtained by capping the Cu trench top with $CoW_xP_y$ metallization. The characteristic EM lifetime is at least as much as 100 times larger than that found for a canonical interconnect at stressing conditions (Aubel *et al.*, 2008; Hu and Rosenberg, 2004; Hu *et al.*, 2004), and given that the CoWP cladding lies over the known fastest global EM path in damascene interconnects, it is clear that significant alteration of the top interface of the Cu metallization




*8.9* TEM cross-sectional image of a Cu interconnect coated with CoWP is shown. Note that the metal cap is also covered by a second dielectric cap. (Reprinted with permission from Hu C-K *et al.,* (2002) copyright 2002, American Institute of Physics.) The image has been digitally enhanced from the original for publication purposes and is probably unsuitable for interpretation of the detailed microstructure.

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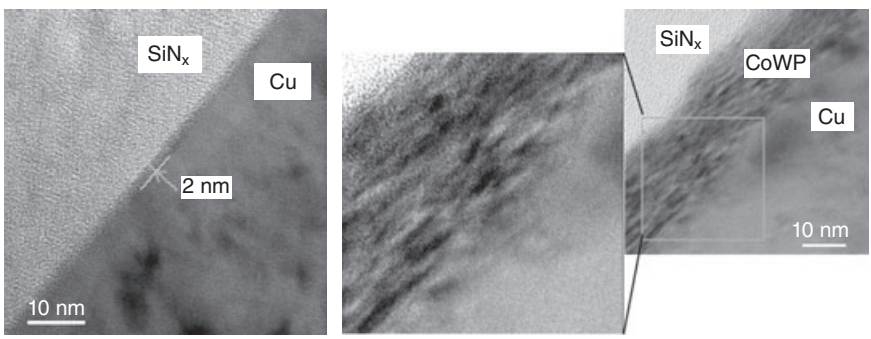
has been achieved to reduce Cu transport and void growth. TEM work by Meyer and Zschech (2007) (see also Zhang *et al.*, 2010a) shows that an interface layer is clearly seen for conventional dielectric cap over Cu, whereas the resulting interface for CoWP capping over Cu is very smooth and nearly epitaxial (Fig. 8.10). Lane *et al.* (2003) have also demonstrated that high interface adhesion strength is achieved so that the $CoW_xP_y$/Cu interface no longer limits EM reliability performance (Lane *et al.*, 2003; Lloyd *et al.*, 2005).

Interestingly, the observed activation energy is observed to be a rather bulk-like 2.0 eV (Hu *et al.*, 2004). To understand this, one can perform some simple calculations. If one assumes a 100 nm line width and interface width of 0.5 nm, then the estimated interfacial atomic fraction is given by $\delta_{cdi}/h \sim 1/100$. If the fraction of atoms at the capping interface is about 1/100th of the number of atoms in the bulk, then a Cu/CoWP interface with activation energy ≥1.8 eV (depending on $Z^*$, $D_0$ values assumed) would be sufficient to mimic the kinetic behavior of Cu self-diffusion (Hu and Rosenberg, 2004; Hu *et al.*, 2004). To estimate, one assumes that the drift velocities of the bulk versus capping interface are the same. Then, one can directly calculate what the activation energy for capping dielectric must be for a given value of bulk activation energy. For the values that assumed in Table 8.2, a capping activation energy as low as 1.3 eV would be sufficient, but again, this value is dependent upon what values are used for the EM parameters. CoWP capping has the added benefit of not significantly increasing the Cu metal resistivity. Although a few percent increase in resistance can be observed




*8.10* (a) TEM cross section of $SiN_x$ capped dielectric over Cu metal is shown. An interface layer about 2 nm thick is visible. (b) In contrast, the TEM cross-section of CoWP capped Cu metallization shows a very smooth transition from Cu to CoWP. The higher resolution inset indicates that regions of near-epitaxial quality CoWP film are generated over Cu. (Reprinted with permission from Meyer and Zschech (2007), copyright 2007, American Institute of Physics.)

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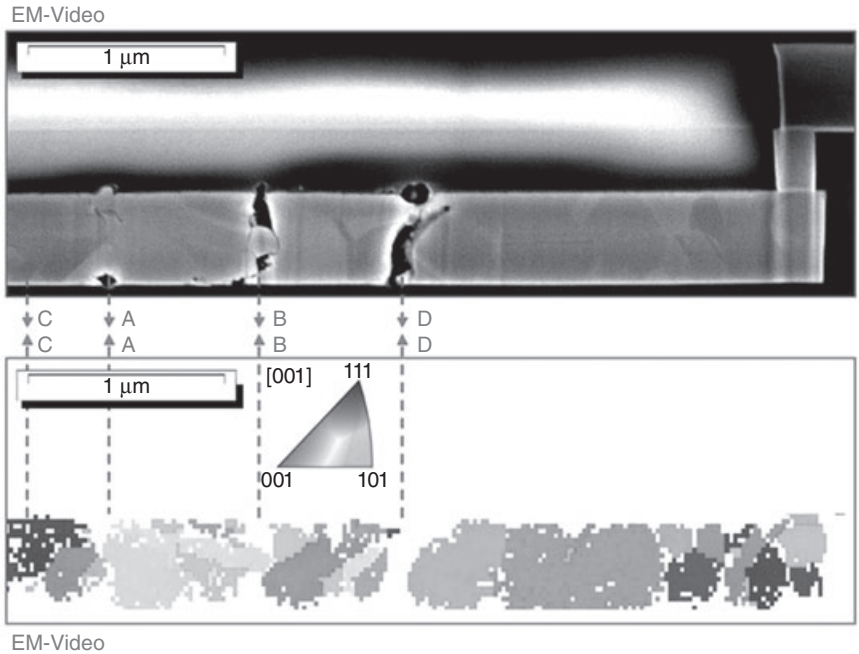
owing to Co diffusion into Cu metal during EM stress at 400 °C (Hu and Rosenberg, 2004; Hu *et al.*, 2004), the magnitude of resistance increase by Co penetration in real-world applications (125 °C or less) would be less significant. *In situ* SEM imaging by Meyer and Zschech (2007) shows that the strong EM resistance of the CoWP capping layer to Cu allows void formation downward across a grain boundary (and across the line width) can be complete enough to cause interconnect failure even if the vertical slit void forms some distance away from the cathode end (Fig. 8.11). The generation of such 'slit-like' voids shows that grain boundary diffusion plays a larger role for strongly capped interconnects. Consequently, microstructural details such as the grain boundary angle to the line direction and type of grain boundary are important characteristics to monitor.

There may be some concern, however, with the integrity of this process against intermetal dielectric breakdown because $CoW_xP_y$ tends to lose its deposition selectivity with decreased spacing between adjacent Cu metal lines (Moon *et al.*, 2009). This loss of selectivity means that protrusions from




*8.11* Post-EM SEM/electron back scatter diffraction (EBSD) analysis of Cu interconnect with CoWP capping shows that slits voids are found at locations where vertical grain boundaries spanned the entire interconnect width. (Reprinted with permission from Meyer and Zschech (2007), copyright 2007, American Institute of Physics.)

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a metal line, small islands of CoWP metal, or poorly capped areas over the Cu metal surface can form after CoWP deposition, which erodes interconnect reliability against low-*k* dielectric breakdown. Despite this concern, process solutions against such risk and with no demonstrable yield impact have been found down to at least the 32 nm node (Gambino *et al.*, 2006; Nopper *et al.*, 2009; Huang *et al.*, 2009; Moon *et al.*, 2009). Furthermore, Co capping using a chemical vapor deposition (CVD) process has been demonstrated (Nakazawa *et al.*, 2008) which may have fewer problems with selectivity loss. Ru capping using selective CVD has also been demonstrated (Yang *et al.*, 2009). Other novel approaches such as usage of an aqueous molecular masking layer to modify the low-*k* dielectric surface to become more hydrophilic are being investigated (Besser *et al.*, 2008). Also, use of $CoW_xB_yP_z$ in the integrated BeoL process must be considered with some care because of an inherent soft error failure risk associated with elemental boron (B) (Baumann *et al.*, 1995). Another road block is the additional cost of implementing electroless plating technology to already existing processes used for canonical Cu interconnect integration (Shaviv, 2008) and would possibly require careful economic calculation in situations where cost control is at a premium.

The more conventional approach by doping the Cu metal (e.g., with Al) is also shown to improve EM (Vanypre *et al.*, 2007; Yokogawa and Tsuchiya, 2007; Yokogawa *et al.*, 2008), although the expected increase in resistivity associated with such doping is a drawback, especially when the intrinsic Cu interconnect resistivity increases with decreasing line width (Tada, 2004). In this scenario, the Cu seed deposited by physical vapor deposition (PVD) and doped with Al is used, and during subsequent processing, the dopant spreads through the grain boundaries and can also spread into the capping interface. Hu *et al.* (2010) argues that Al doping actually arrests interface diffusion and is less effective against grain boundary EM (Michael and Kim, 2001). A variant using a CuMn seed alloy is shown to have similar benefits, and in addition, it is more compatible with lower resistivity metal liners such as Ru and Co (Nogami *et al.*, 2010a). A Ti/TaN barrier layer doping scheme where $TiO_x$ reactant formed after Ti gettering of low-*k* oxygen or moisture within low-*k* enters into the grain boundaries to lessen grain boundary migration has shown promising results (Hamada *et al.*, 2010). Interconnect line or via resistivity impact is not mentioned however. A strong EM performance benefit by using a Ti liner as a dopant source has also been demonstrated but with a resultant resistivity increase penalty (Kakuhara *et al.*, 2010). Use of Co as a part of the metal liner has shown good EM results because Co has presumably diffused into the grain boundaries (Nogami *et al.*, 2010b). One other variant is the combination of SiGe surface preparation along with CuAl seed process to improve the reliability margin (Shaviv *et al.*, 2008).

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An alternative method to improve EM is the generation of an interface layer that allows stronger adhesion of conventional dielectric capping to trench top. Silicidation of the trench top interface (Lin *et al.*, 2004, 2005; Chattopadhyay *et al.*, 2006; Usami *et al.*, 2006) is a promising approach because the EM performance enhancement is about two- to threefold, and the approach is attractive because it requires little modification from the processes used already (positive cost-benefit); however, there is a performance penalty owing to the resistivity increase from Si penetration into the Cu metal. Therefore, to take advantage of this approach, precise control of the interface is needed to benefit from improved EM performance without sacrificing the resistivity increase to an unacceptable extent. An alternative approach using $SiN_x$ film precursor gas without significant resistivity fall-off has been demonstrated; however, the EM performance benefit remains somewhat modest at a threefold improvement over a canonical reference process (Le-Friec *et al.*, 2009) under EM stress conditions. A $SiGe_xN_y$ process also shows promise with a relatively modest 5% resistance increase and about a fourfold lifetime improvement under EM stress conditions over a canonical reference process (Liu *et al.*, 2008). Work by Hohage *et al.* (2009) has shown that careful silicidation pretreatment of the exposed Cu surface before capping by a dielectric barrier can result in strong EM performance (3.5 times compared with a canonical reference under stress conditions) with less that a 2% increase in resistivity owing to the creation of an epitaxial $CuSi_x$ layer sandwiched between the Cu and capping dielectric. Interestingly, the approach is also shown to negate the trending found between adhesion strength and interfacial EM activation energy because the adhesion between the $CuSi_x$ and the capping dielectric can be rather low compared with a canonical Cu interconnect with a $SiC_xN_y$ capping process. Because the EM mass transport interface is effectively blocked by the epitaxial $CuSi_x$ layer, interfacial quality between $CuSi_x$ and $SiC_xN_y$ is then not relevant for EM performance. The silicidation process has also been combined with a MgO self-forming barrier process (Koike and Wada, 2005) to increase the EM margin substantially (Kudo *et al.*, 2008); however, the MgO barrier does not leave a conductive liner at the via bottom so that use of the Blech effect in design is obviously not possible (Nogami *et al.*, 2010a). Finally, utilization of silicide capping with a Ti barrier metal appears to provide an increased EM margin (~100 times compared with a canonical reference in under stress conditions), and for narrow interconnects less than 100 nm, Ti and Si penetration into the line appears to prevent the occurrence of a severe resistance increase penalty due to alloying to Cu metal. The drawback, however, appears for wider interconnects (>130 nm) which do suffer a significant resistance increase compared with the use of Ta-based barrier metal. A later combination of the above with a controlled amount of surface copper oxide to prevent Si

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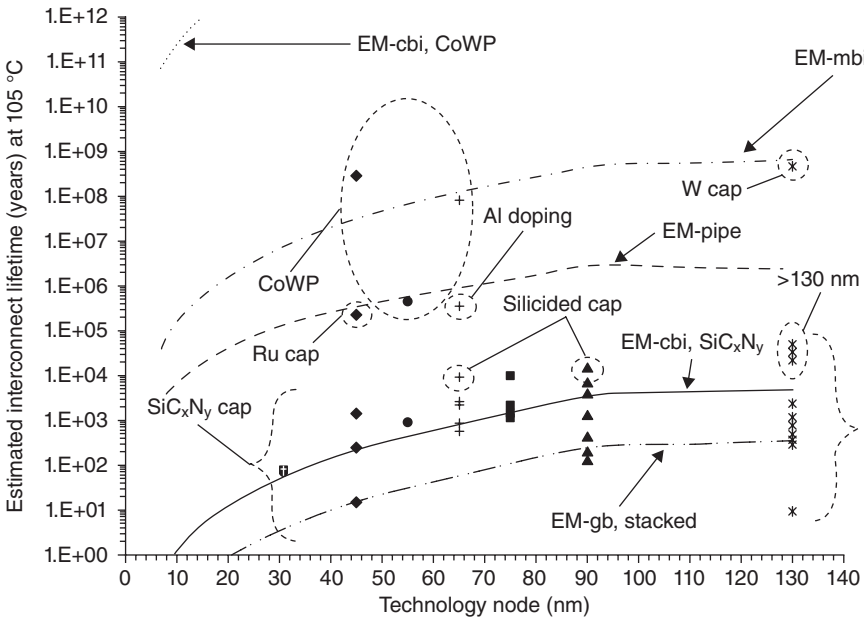
penetration into grain boundaries, provided further improvement (Hayashi *et al.*, 2009, 2010).

Given this need to improve the EM performance margin through some form of interface engineering, it is instructive to see how EM has been tackled in research and to see how the drift model shown in equation [8.6] can fit the reliability trending. The results are shown in Fig. 8.12. The median time-to-failure for different EM pathways at 105 °C are found using EM parameter values taken from Table 8.1 (ITRS, 2009) and from the EM




*8.12* Expected lifetime trending using ITRS-2009 parameters and reported data on diffusion and kinetic parameters for Cu EM is shown along with data on EM lifetimes projected to a single condition at 105 °C. The data show reasonable agreement with expected values and also illustrate the increased EM lifetime advantage for recently developed methods to improve on capping interface quality. Metal capping EM extrapolations may be somewhat optimistic because microstructure impact is not quantified. Data points were obtained from Cheng *et al.* (2006), Croes *et al.* (2010), Hamada *et al.* (2010), Hartfield *et al.* (2004), Hohage *et al.* (2009), Hu *et al.* (2003, 2007a), Kakuhara *et al.* (2010), Leaming-Sphabmixay *et al.* (2007), Lee *et al.* (2005), Lin M *et al.* (2004, 2005, 2009, 2010), Lloyd *et al.* (2005), Ogawa *et al.* (2002), Pyun *et al.* (2005), Rosenberg *et al.* (2000), Saito *et al.* (2004), Tada *et al.* (2004), Wang *et al.* (2005), Yang *et al.* (2009), Yokogawa and Tsuchiya (2004, 2007), Zhang *et al.* (2010b), Zschech *et al.* (2009).

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parameters in Table 8.2. Overlaid on top of these trend curves, a compilation of median EM lifetimes reported are shown. There is a reasonable amount of EM data available, but most of the data is virtually useless for such comparisons because of the sparseness of the details provided. Figuring out lifetime values for extrapolation to a single usage condition is thus quite messy because authors are generally reluctant to divulge specific details of their EM results, typically plotting data using arbitrary lifetime units and not explicitly stating their test conditions (no failure criterion, no current density value, no current exponent, no temperature, etc.) and test structure details (no width, no length, no thickness, etc.). In some cases, the details were not so vague, so some extrapolation was possible, provided certain generic conditions for EM parameters were used to perform the lifetime extrapolations. For example, the activation energy of 0.9 eV and a current exponent of one were used when no equivalent value was provided for each. When such details were provided, however, those values were used. Errors in the extrapolations and a large spread in the results are inevitable, but the extent of the errors lies somewhere near unity. The extracted values (miraculously) appear to match the lifetime projection for a capping dielectric interface without wildly excessive variation. The expected lifetime trending with technology scaling appears consistent with the lifetime extrapolations of the literature data. The result also generally agrees with the trending found by Croes *et al.* (2007), where it is predicted that canonical interconnect EM will be suitable down to the 32 nm node. The trends shown in Fig. 8.12 seem slightly more pessimistic because the median life is plotted instead of the 100 ppm projection used by Croes *et al.* Croes *et al.* also assumed a higher current exponent of 1.2, which would decrease further his projected lifetime compared with that of Fig. 8.12. Furthermore, the interface engineering approaches to EM improvement do seem to provide a substantial EM margin that is well above the noise of the EM lifetime projections for the canonical pathway model. The presence of stacked grains in the EM pathway is truly a fast EM pathway, and it will be critical to ensure that such pathways are not extensive (continuous and long) and not present around vias, even when the interface engineering methods have been implemented (Lin *et al.*, 2010). Vias are the most vulnerable location for EM failures because they are necessarily placed at the interconnect ends. Results by Arnaud *et al.* (2010) with regards to interconnect early failures seem to mirror this concern. Finally, as a caveat, Lin *et al.* (2010) using a statistical-based approach to combine the effects of bamboo and polygranular segments provided estimates of the $Z^*D_0\delta$ products for interface and grain boundary EM along with their respective activation energies. The $Z^*D_0\delta$ product values differ substantially from the corresponding product values used in the above calculations. In this instance, the difference appears not to have made a large impact because the calculations in Fig.

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8.12 assumed that the grain boundary diffusion was rate-limited by interface diffusion; i.e., that the grains were fully columnar. Of course, discrepancies would probably be more obvious when more detailed or direct EM data are examined. However, the comparison does point to the dangers or difficulties in trying to construct a detailed analysis of EM trends from disparate literature resources.

The ability to improve the interface properties at the trench top has increased industry confidence in meeting reliability needs for future scaling; however, there is a complication to this picture. It is clear that, as the critical feature size continues to shrink, it is becoming increasingly difficult to effectively control the microstructure within the Cu trenches. The grain structure shows greater degrees of polygranular character within the trench for interconnects beyond the 65 nm node (Hinode *et al.*, 2001; Hu *et al.*, 2007b) so an increasing contribution from the grain boundary pathway is expected and this may be the limiting factor for EM performance (and resistivity improvement) in future. Unless practical methods (i.e., manufacturable) to increase the grain size for the narrowest leads are invented, approaches to improve EM performance through metal doping may be needed to provide additional EM margin but at the expense of additional resistivity increase (Yokogawa *et al.*, 2008).

## 8.4 Copper microstructure impact

### 8.4.1 Microstructure development in damascene copper interconnects

The microstructure that develops in Cu damascene interconnects is greatly affected by a number of process-related factors, including etch profile and uniformity (Choi *et al.*, 2010), barrier/seed deposition, ECD conditions such as the impact of impurity concentration (Neuner *et al.*, 2010), anneal conditions (Barmak *et al.*, 2003; Brandstetter *et al.*, 2010; Carreau *et al.*, 2007), defect generation (Detavernier *et al.*, 2003), overburden thickness (Dubreuil *et al.*, 2008; Field *et al.*, 2003), and metallization stress or strain (Harper *et al.*, 1999). The main factors affecting grain size within a damascene trench, however, are the interconnect dimensions (Besser *et al.*, 2001; Brandstetter *et al.*, 2010; Cho *et al.*, 2005; Lingk *et al.*, 1999; Vanasupa *et al.*, 1999b; Wu *et al.*, 2004). The as-plated grain size is small, somewhere on the order of 50 to 100 nm, and depends on the plating conditions used. Generally, the most characteristic film texture for as-deposited and annealed Cu films is (111)-oriented with contributions from other secondary grain orientations such as (200) and (311) (Cho *et al.*, 2005; Lee *et al.*, 2003; Neuner *et al.*, 2003; Rosenberg *et al.*, 2000; Vanasupa *et al.*, 1999a). The microtexture found in Cu interconnects has a much less preferred orientation (Ji *et al.*, 2004) than

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that in Al metallization found in microelectronics (Rosenberg *et al.*, 2000). In Cu lines, (111) oriented grains from the trench bottom and sidewalls are found (Besser *et al.*, 2001; Cho *et al.*, 2005; Ganesh *et al.*, 2010). A (111) oriented fiber texture is considered advantageous for grain boundary EM for Al(Cu) metallization (Knorr and Rodbell, 1996; Knorr *et al.*, 1991) and has been confirmed for Cu metallization (Abe *et al.*, 2004; Ryu *et al.*, 1999); however, developing the preferred (111) orientation trenches within ultra-narrow trenches is difficult to achieve because side-wall grain growth is prevalent (Leaming-Sphabmixay *et al.*, 2007). For wider interconnects (>~0.5 μm), the grains tend to be polygranular so that smaller grains bunched together can span a given line width. The presence of the overburden has a stronger effect on the microstructure development within wider trenches so that grains can extend from the trench bottom to the overburden surface. The grain boundaries in such instances tend to be more or less vertical, but if several grains are needed to span the interconnect width, a clear longitudinal grain boundary EM pathway would exist for extended lengths over large sections along the interconnect.

When the interconnect line width is reduced, the overburden is found to have limited relation to microtexture development within the trench (Besser *et al.*, 2001; Brandstetter *et al.*, 2010) below 250 nm and virtually no effect at 80 nm or less, although its effect may be more pronounced when the overburden is purposely reduced (Dubreuil *et al.*, 2008). For a narrow interconnect, sidewall growth is thought to increasingly lead to greater complexity in the microstructure (Besser *et al.*, 2001); however, it has recently been argued that a superconformal filling process (Andricacos *et al.*, 1998; Josell *et al.*, 2001) may limit such sidewall orientation contribution for interconnects with widths at least down to 140 nm, especially after thermal anneal treatment. Furthermore, it is argued that stress profiles along the length and depth of the trench during anneal have a greater impact on the final texture than sidewall growth (Cho *et al.*, 2005). As for grain size, it scales roughly with the interconnect width so that, for the narrowest interconnects (80 nm and below), the grains can be longer than wide (Graham *et al.*, 2008); however, it is also found that the interconnect grains show regions of bamboo and polygranular character with smaller grains found deeper in the trench than higher in the trench (Hu *et al.*, 2007b). Interestingly, electrochemical deposition (ECD) actually yields a larger grain size than other deposition methods such as physical vapor deposition (PVD) or chemical vapor deposition (CVD) (Ryu *et al.*, 1999). Twinning is evident in Cu grains regardless of the line width, although the grain size increases and twinning density decreases after thermal anneal treatments (Cho *et al.*, 2005; Hübner *et al.*, 2010). Grain boundaries defined by twins generally have low energy so that they are very unlikely to be effective pathways for EM mass transport (Chen *et al.*, 2008b).

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Brandstetter *et al.* (2010) has shown that high temperature annealing (400 °C for 6 h) has a pronounced effect (16-fold increase with overburden) on grain size only for the larger width interconnects, and a lower temperature anneal (150 °C for 6 h) has somewhat less effect (10-fold). Below 250 nm, the annealing impact on grain size is less significant even for 400 °C annealing (70 nm increased to 100 nm at 80 nm line width). The resulting changes to the microstructure appear to reduce the overall strain present within the Cu grains (Lingk and Gross, 1998; Harper *et al.*, 1999; Moriyama *et al.*, 2003; Lee *et al.*, 2003; Ito *et al.*, 2007); however, the overburden-driven strain energy minimization process of grain growth is stunted by the presence of the interconnect side walls (Wu *et al.*, 2004). When considering such general trends, however, one should be aware that the microstructure found in actual production environments depends upon the explicit process flow used and is not necessarily optimized for grain size or microtexture uniformity.

### 8.4.2 Microstructure impact on copper EM

When EM is rate-limited by interface mass transport, as is the case for canonical damascene Cu, little evidence of microstructure impact on EM will be apparent (Arnaud *et al.*, 1999; Hu *et al.*, 1999a; Hau-Riege and Thompson, 2001). Hau-Riege and Thompson ran an interesting experiment where direct alteration of the microstructure using a scanned laser annealing method yielded little difference in EM performance in 500 nm wide interconnects. It should be noted that these results pertain to intermediate width interconnects, where the overburden grain growth can extend deeper into the trench. In such intermediate width interconnects, the grain microstructure is found to exhibit bamboo or near-bamboo character (Hu *et al.*, 2007a; Brandstetter *et al.*, 2010). Thus, changing the microstructure for such an interconnect could possibly mean a change from a smaller density of shorter length bamboo grains to a larger density of longer ones. Ryu *et al.* (1999) did find differences in EM performance in Cu CVD-deposited long test lines with larger dimensions (1.5 μm width and 0.5 μm thickness). It was found that the (111)-preferred orientation had a four-fold better EM performance than the (200) oriented test lines so that some microstructure effects are likely present. In this instance, the test lines would be expected to show polygranular character, especially since the deposition method is CVD and not ECD, so that a microstructure dependence seems reasonable. These CVD metal lines, however, were not passivated, and the effects observed may have been manifested by differences in surface diffusion along differently oriented grain surfaces (which is maybe a more subtle microstructure effect). In summary, the natural conclusions are the following: (a) for wider polygranular interconnects (more than 1 μm), one would

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expect to have significant contributions from both interfacial and grain boundary EM; (b) for intermediate width interconnects (say, 200 to 3000 nm width), Cu grain boundaries in ECD-deposited interconnects do not matter so much after annealing. Such microstructure is not as important because (i) they are not able to form fast percolative pathways throughout the interconnect length [perhaps because they are blocked by individual bamboo grains or maybe width spanning twinned grains (Hübner *et al.*, 2010)] or (ii) the interface pathway is much faster than any grain boundary pathway even when a percolative path exists. Regardless, any means of increasing the interface pathway resistance to EM increases the influence of the grain boundaries on EM performance as Hau-Riege and Thompson astutely noted in 2001 before the described methods of capping interface improvement were introduced. Similar conclusions have been formed by Ogurtani and Oren (2001) using a more theoretical analysis.

For much narrower interconnects, the grain size may have a clearer role because they probably define the vertical component of the critical void volume, equation [8.5] for EM failure (Arnaud *et al.*, 2010; Li *et al.*, 2004; Oates and Lee, 2006). Thus, the presence of small grains within and under vias may set the conditions for EM early failures. Furthermore, polygranularity in narrow interconnects probably enhances the role of grain boundary diffusion during EM (Hu *et al.*, 2007a, 2010). Then, when interface engineering to arrest interface EM is implemented, the role of grain boundary formation in void nucleation and growth is enhanced (as is evident from Fig. 8.11). Recent observations confirm that EM in CoWP-capped interfaces does not provide as large an EM margin as expected if extended grain boundary paths exist (Hu *et al.*, 2010; Zhang *et al.*, 2010a, 2010b). Hence, microstructure control, and not just interface engineering, is absolutely vital to retain an EM margin in well-capped interconnects below the 32 nm node (Lin *et al.*, 2010).

If grain boundary EM does become a more critical factor, then presumably much of the learning from grain boundary EM in Al should find relevance. Suo *et al.* (1994) have shown that circular voids will preferentially follow an instability located on a hemispherical void during EM stress so that the instability is extended in opposition to the healing forces owing to surface energy (void surface tension). In contrast to maybe an interface dominant situation but under the same types of EM and surface tension effects, the voids would be expected to extend along the current flow direction (Choy and Kavanagh, 2004). In this context, a grain boundary that connects to an interface is a natural generator of local instability, should a hemispherical void pass through it (Zaporozhets *et al.*, 2005), and such void growth and void translation physics appears to be similar to what is observed by *in situ* SEM studies (Meyer and Zschech, 2007). Stress modeling of the microstructure effect on void nucleation indicates that small grains at an

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interface may be susceptible to fracture and are candidates for void nucleation events (Kteyan *et al.*, 2007). Hau-Riege *et al.* (2004) showed that the critical stress for void nucleation decreases as the Young's modulus of the surrounding dielectric decreases and has implications for scaling with the need to incorporate ultra-low-*k* dielectrics or air gap technology and reduced metal barrier thickness. Because grain boundary triple points remain at the capping interface, voids probably nucleate there (Vairagar *et al.*, 2004b), especially at non- $\Sigma 3^n$ boundaries that intersect an interface wall (Arnaud *et al.*, 2006; Cayron, 2007). Grain boundary triple points within the metal may also become important sites for void nucleation too. When a grain boundary EM pathway begins to dominate (at least locally around the grain boundary), voids can grow along the grain boundary and generate width spanning slit voids (Sukharev *et al.*, 2009). Ogurtani and Oren (2004) developed a detailed model of void dynamics occurring in bamboo-type interconnects and identified a time-to-failure equation based on the average number of bamboo grains that need to be passed before a given fatal void reaches the cathode end.

Not all grain boundaries provide sufficiently fast EM pathways and, at present, detailed analysis has not been done to identify those grain boundaries that are most susceptible to forming trans-width slit voids. From Al-based EM (Hu *et al.*, 1995), it is expected that (111) tilt grain boundaries with low misorientation angles (<11° to 15°) are poor pathways for EM voiding. High-angle misorientation boundaries probably provide faster diffusivity paths with the exception of certain special boundaries known as 'coincident site lattices' (CSL). Because Cu is also an FCC metal, similar arguments would be expected to apply; however, for Cu damascene interconnects, the Cu lines do not show as strong (111) fiber texture so that a higher density of grain boundary pathways should be active. Thus, more detailed analysis will be needed.

More pragmatically, if horizontal or vertical slit voids only form well beyond the expected life for microelectronics devices under regular use conditions, then the detailed microstructure EM physics is only a minor concern to those more interested in simply meeting the performance demands of the ITRS roadmap. The question remains whether such a reliability margin can be met by the billions of interconnects undergoing some degree of EM amount in a customer environment. To address those concerns, more detailed statistical analysis to identify the extent of EM early failures is necessary. Such discussion, however, is beyond the scope of this chapter, but suitable references are provided because it is an important topic (Gall *et al.*, 1997; Hauschildt *et al.*, 2007, 2008; Lee and Ho, 2004; Li *et al.*, 2006; Oates and Lee, 2006; Ogawa *et al.*, 2001; Tsuchiya and Yokogawa, 2006). Layout effects on EM are also an important consideration and are also listed for reference (Girault *et al.*, 2008; Hau-Riege and Klein, 2008;

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Hau-Riege and Thompson, 2000; Kakuhara *et al.*, 2009; Park *et al.*, 2010; Roy *et al.*, 2009).

## 8.5 Conclusions

Although the basic integration scheme has remained the same since the first implementation of Cu metallization into advanced CMOS technology, significant evolutionary improvements have been found to increase the EM reliability margin so that Cu interconnects probably remain the interconnect of choice well-beyond the 22 nm node. Such adjustments to the canonical integration scheme for Cu interconnects are necessary to keep pace with the performance demands from dimensional scaling. Dimensional shrinkage, resistivity increase, and increased current density requirements are key technology drivers that are steadily eroding the EM reliability margin by roughly 50% per technology generation. Key to these evolutionary changes are the different methods of interface engineering to be used to stop the mass transport pathway at the top interface of the Cu damascene trench, although increased contribution from grain boundary pathways should arise and may reduce the expected reliability margin. Such improvements must be achieved without seriously contributing to the expected increase in Cu metallization resistivity with dimensional scaling from increased grain boundary and interface scattering effects. The EM contributions from grain boundary diffusion pathway in ultra-narrow interconnects cannot be dismissed because narrow void failures have been observed and will place greater demands on the ability of redundant metal liners to maintain current carrying capabilities should such catastrophic slit voids develop. Thus, unless an optimal balance between interface and microstructure control is obtained but not at the expense of increased intrinsic Cu resistivity, the EM reliability margin under dimensional scaling pressure will steadily erode to an unacceptable level of intrinsic reliability performance. Even with these changes and with the expected difficulties in finding alternative metallization schemes that provide the same magnitude of manufacturability yet improved interconnect performance, Cu metallization is the foreseeable choice for interconnect technology at least to the end of this decade.

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# 9

# Electromigration-induced microstructural evolution in lead-free and lead–tin solders

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**Abstract**: The electromigration-induced microstructural variation at the joint interface and within the bulk of Pb-free and Pb–Sn solders is examined. The accumulation of solder alloy elements accelerates the interfacial reaction and thus the formation of interfacial intermetallic compound. The formation of intermetallic compound results in stress accumulation and enhances whisker growth within the solder. The torque induced by electron wind results in grain rotation of the solder bulk. The current stress causes the dissolution and thus supersaturation of second phase in the matrix, for example Zn in Sn of a Sn-Zn solder. Dissolution and thus recrystallization of the second phase occurs. The recrystallization behavior of the second phase has been observed for Sn–9Zn.

**Key words**: solder microstructure, intermetallic compound, whisker, hillock, recrystallization.

## 9.1 Introduction

A number of factors affect the microstructure of material. The variation in composition of a material gives rise to diffusion upon thermal aging owing to chemical potential. Diffusion results in the dissolution of alloying elements in the matrix and thus diminishing second phases. Diffusion also enhances interactions among constituent elements and thus the formation of compound such as intermetallics. The momentum transferred from electrons to atoms during current stressing causes migration of the atoms and thus the occurrence of electromigration, a directional forced atomic movement (Huntington, 1975). The elemental diffusion owing to chemical potential in conjunction with the electron wind force owing to electric current raises the energy level of the atoms in a metallic material. Consequently, there are a variety of interactive behaviors occurring induced by electromigration. In view of the excess energy impinged by the electric current, it is reasonable to anticipate further behaviors other than those caused by the conventional diffusion process. In addition, the heterogeneity in lattice and properties of the solder alloy, compared with the homogeneous property of pure metal like Al and Cu, further causes complexity to the microstructure variation during electromigration. The well recognized Black's equation



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also needs appropriate amendment to accommodate the complexity of solder alloy (Choi *et al.*, 2003). The accelerated failure, faster than the mean time to failure (MTTF) predicted by Black's equation, of a solder joint resulted from a combination of current crowding, dissolution of IMC, and Joule heating (Choi *et al.*, 2003). The major occurrences reflected in microstructure variation include phase separation, compound formation, grain extrusion and rotation, whisker and hillock formation, void nucleation and growth, recrystallization of second phase, and lattice reorientation. These occurrences together result in the formation of defects and accelerated failure of the electronic components.

## 9.2 Intermetallic compound formation

The atomic flux in a metallic material under the influence of electric current stressing is given by the Nernst–Einstein equation. This is the flux of the atoms traveling through the bulk under the influence of electric field. However, the electric field and the current flow induce a polarity effect on the electrode which causes different intermetallic compound (IMC) formation behaviors to cathode and anode, Fig. 9.1 (Wu and Chan, 2005). The thickness of IMC layers formed in diffusion couples such as Cu/Sn and Ni/Sn (Chen *et al.*, 1998) is governed by the electric current. For Sn–Pb solder, the Pb atoms move in the same direction as the electron flow, whereas the Sn atoms move in the opposite direction. A 97Pb3Sn solder bump thus becomes 83Pb17Sn in the cathode region (Nah *et al.*, 2004) at a current density of $2.55 \times 10^4$ A cm$^{-2}$ and causes the formation of $Cu_6Sn_5$ IMC. The electric current does not result in significant change to the initial anodic compound formed after reflow.

Nevertheless, the consumption of cathodic electroless nickel under bump metallurgy (UBM) was accelerated to form $Ni_3Sn_4$. Current stressing at an average current density of $0.4 \times 10^4$ A cm$^{-2}$ at 25 °C through a Sn0.7Cu ball grid array (BGA) package causes complete dissolution of the Au/Ni (5 μm thick) UBM and the 17 μm Cu pad (Zhang *et al.*, 2008). The current density increases up to $5.83 \times 10^4$ A cm$^{-2}$ in the current entry corner area. Ni forms the Ni–Sn IMC $Ni_3Sn_4$ in the nearby area. The formation of the IMC was partially attributed to the inevitable temperature rise as a result of Joule heating owing to current crowding at the entry corner. Meanwhile, the unprotected Cu pad dissolved rapidly in the solder and flowed to form $(Cu,Ni)_6Sn_5$ at the anode area.

In a μBGA (300 μm diameter solder ball) 63Sn37Pb solder joint with Cu UBM on the component side, the IMC $Cu_6Sn_5$ and $Cu_3Sn$ were formed. The thickness of the IMC depends on the current direction as a result of polarity effect (Alam *et al.*, 2006). The IMC is thicker when the component acts as the anode, with a current density of $1.3 \times 10^4$ A cm$^{-2}$, whereas it is thinner

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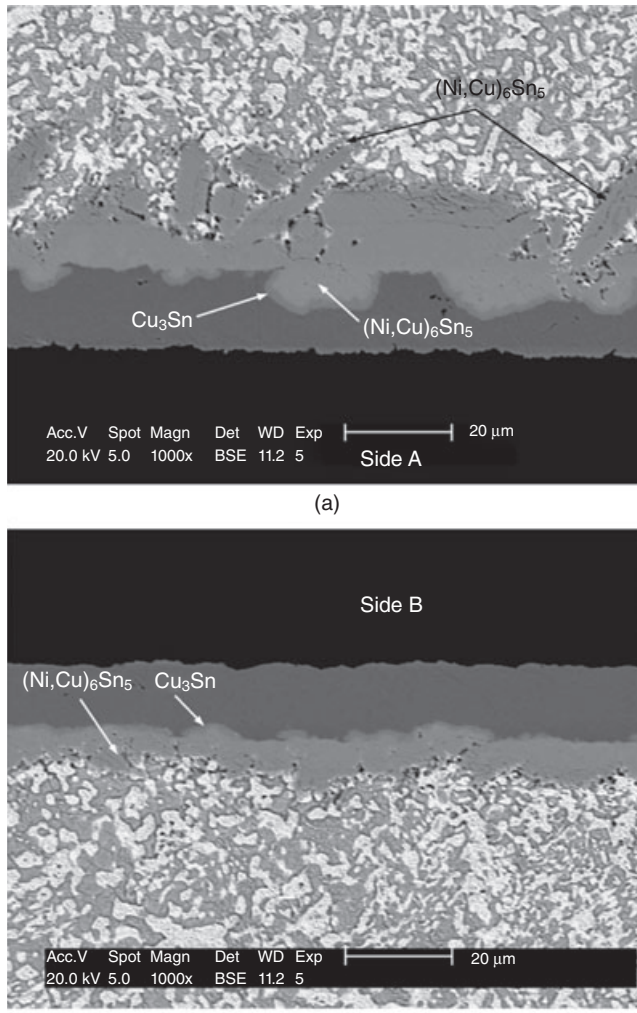


*9.1* The polarity effect during current stressing causes different reaction behavior at (a) the anode and (b) the cathode. The 63Sn37Pb BGA solder joint was stressed with 1.5 A for 11 h (Wu and Chan, 2005).

when it is the cathode. Similar occurrence was observed for the $(Cu,Ni)_6Sn_5$ IMC formed on the boardside where electroless Ni–P was applied as the barrier layer. Temperature enhances the IMC growth. Electric current stressing at higher temperature, 150 °C versus 20 °C, significantly accelerated the IMC growth even operated at lower current density, $9 \times 10^3$ A cm$^{-2}$ versus $1.3 \times 10^4$ A cm$^{-2}$. The polarity effect on IMC growth may be affected

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by the testing structure and the Cu concentration in the solder joint. The polarity effect was prominent in a stripe structure with Cu/Sn–3.8Ag–0.7Cu/Cu system (Gan and Tu, 2002), but not in a Ni/Sn–Ag/Cu system (Ebersberger *et al.*, 2005).

In a Cu/Sn–3Ag–0.5Cu/Cu solder bump system with Cu pad, replacing the Ni/Au finish in both the anode and the cathode areas accelerated IMC growth upon current stressing at $10^4$ A cm$^{-2}$ at 180 °C (Yamanaka *et al.*, 2007). The current stressing enhances the thickness growth of $Cu_6Sn_5$ more than $Cu_3Sn$. Yet the enhancement in IMC growth is retarded when there are voids formed which interrupt the Cu transport. The polarity effect also stops when the Cu concentration in the solder bump reaches a certain level after current stressing. In addition to the polarity effect, current circulation through the bump enhances IMC growth at the bottom of the joint even when the current was not passing through it owing to the structural design of the component (Yamanaka *et al.*, 2007). The polarity effect in a Ni(P)/SnPb/Ni(P) BGA package shows fast depletion of Ni and Cu at the cathode but it enhances the growth of $Ni_3Sn_4$ at the cathode and $(Cu,Ni)_6Sn_5$ at the current crowding triple point (Lu *et al.*, 2009a). The effect of current stressing on IMC growth was probably suppressed by alloying element. The addition of 0.6% Zn in Sn–Ag solder attracts Cu elements and surpasses the current influence on Cu transport. The addition of Zn stabilized the $Ag_3Sn$ and $Cu_6Sn_5$ IMC in the solder joint under current stressing and gave rise to better reliability than Sn–Ag solder having up to 1.8% Ag (Lu *et al.*, 2009a). The dissolution of cathode metallization produces an atom flux toward the anode as pushed by the current stressing. The atom flux may not completely reach the anode as the atoms may be trapped during the flow towards anode. The Au metallization of the cathode side in the Cu/Au/SnAgCu/Cu combination dissolves rapidly during the current stressing at $10^3$ A cm$^{-2}$ at ambient temperature. The solder matrix contains longitudinal $Cu_6Sn_5$ after reflow. It is of interest that the Au forms $AuSn_4$ which precipitates at the tip end of the longitudinal $Cu_6Sn_5$ IMC after 72 h of current stressing, Fig. 9.2 (Chiu and Lin, 2008). It is apparent that the formation reaction of the Au–Sn IMC takes place in the path of Au flux. The tip of the Cu–Sn IMC, owing to its high surface energy, serves as the nucleation site for the $AuSn_4$ IMC.

## 9.3 Void formation

In a metallic material, voids may form through a variety of mechanisms and thus affect the mechanical properties and physical properties of a material. In addition, the formation of voids in the solder joint of an electronic component affects the reliability in use. The formation of voids in a metallic material, apart from those formed by poor manufacturing, is generally

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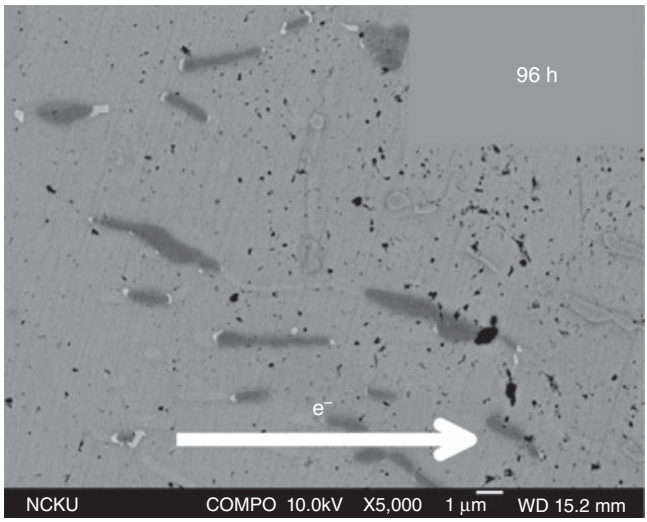


*9.2* The Au flux from the dissolution of the metallizaton layer reacts with Sn of the Sn4Ag0.5Cu to form $AuSn_4$ IMC (white precipitate at the tips of the $Cu_6Sn_5$ IMC) and precipitate at the tips of the $Cu_6Sn_5$ IMC (dark precipitate) (Chiu and Lin, 2008).

induced by an unbalanced atomic diffusion flux. The Kirdendall void forms after prolong unbalanced atomic counter diffusion at the interface between two contact phases. The counter diffusion occurs as a result of the chemical potential difference between the two phases.

Electromigration, however, receives contributions from chemical potential and electron wind force. The electron wind force, induced by electric current, is the factor that accelerates the atomic flux. The migration of atoms away from an interface causes depletion and thus void formation if there is insufficient supply. The electron entry in a solder joint is a typical location for void nucleation and growth (Yeh *et al.*, 2002). There is no solder constituent supply from the chip or substrate side during electric current stressing.

In a flip chip eutectic SnPb solder bump structure, void nucleation occurs at the corner of current entry after an incubation period of 30–50 min with $4 \times 10^4$ A cm$^{-2}$ at 30 °C (Lin *et al.*, 2005). The void nucleation initiates at the corner as a result of current crowding and thus Joule heating. The void exists between the $Cu_6Sn_5$ IMC and solder. During current stressing, the IMC initially formed upon reflow dissolves and new IMC forms with the Cu supplied from the UBM. The electric current detours and moves forward to the front of the void, thus forcing the void to grow. The void grows and propagates rapidly along the UBM/solder interface after nucleation. Thermomigration does not show a significant contribution to the void

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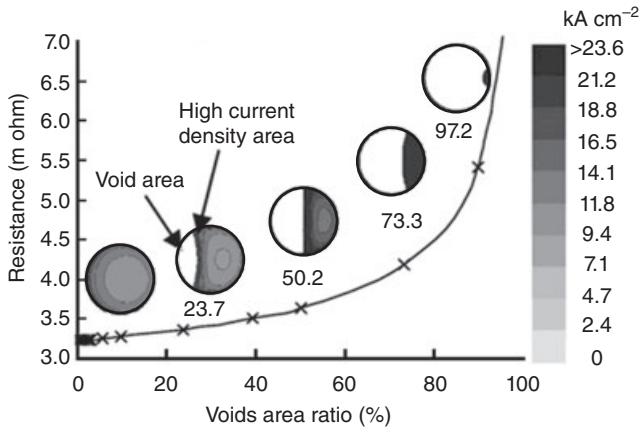
growth. Nevertheless, the formation of void increases local resistance and thus a fast temperature rise that causes melting to the solder (Lin *et al.*, 2005).

Voids also formed at both the IMC/solder and the UBM/ IMC interfaces in a flip chip BGA using Sn3Ag1.5Cu solder with Ti/NiV/Cu UBM when stressed at current density $1 \times 10^4$ A cm$^{-2}$. The extent of voids formed at the solder/IMC interface near the substrate side depends on the metal finish. Ni exhibits a slower dissolution rate in solder than Cu. There it tends to form more voids with the Cu/Ni/Au metal finish than with the Cu-OSP pad when the substrate serves as cathode (Jen *et al.*, 2009).

The behavior of void formation was also reported to occur at the low current density side of a Cu/Sn/Cu solder bump joint. A high current density at the current entry corner of this structure consumed more Cu UBM which caused high Cu concentration and thus the extensive formation of IMC. On the other end of the same Cu UBM, however, the relatively low current density did not raise the temperature significantly. Consequently, the void was formed at the cathodic IMC/solder interface in contact with the Cu UBM (Tseng *et al.*, 2010).

The void growth was simulated and studied with a flip chip solder joint Cu/Sn–3Ag–0.5Cu/Cu system, Fig. 9.3 (Yamanaka *et al.*, 2007). In this system the Kirkendall voids were observed at the Cu/$Cu_3Sn$ interface. However, the void induced by current stressing nucleates at the solder/$Cu_6Sn_5$ interface. The finite elemental simulation of void propagation was conducted with a specific focus on its rate at the currently entry side but without consideration on Joule heating. According to the result of simula-




*9.3* A simulated resistance change for a joint with respect to void area ratio. A high current density area exists in the front of the void progress (Yamanaka *et al.,* 2007).

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tion, a high current density front edge exists between the void area and the residual layer. The current density can increase up to four times the initial value. The joint resistance increases in proportion to the void area ratio increase. The formation of void at the electrode causes an increase in local resistance and thus a temperature rise. A higher temperature also accelerates void formation and growth. The propagation of the void across the entire interface results in an abrupt jump in the voltage as observed for a Cu/42Sn–58Bi/Cu structure (Guo *et al.*, 2009). The accumulation of voids after prolong current stressing gives rise to the interfacial crack. The void itself may be regarded as an accumulation of vacancy flux driven by current stressing. The void serves as the vacancy sink and helps to keep the vacancy at thermal equilibrium during current stressing across a Cu/Sn–3.0Ag–0.5Cu/Cu joint at a current density of $4.9 \times 10^3$ A cm$^{-2}$ (Kinney *et al.*, 2009). Void formation also correlates to the activation of electromigration. The activation energy, 0.84 eV, of electromigration in eutectic SnAg solder bump with Cu-Ni UBM is related to void formation, although it is related to IMC formation when Cu UBM was used for eutectic SnAg and SnPb solder bumps (Chen and Chen, 2010). In a Cu/Sn9Zn/Cu structure the void forms at the $Cu_5Zn_8$ IMC/solder interface when the current density is $10^3$ A cm$^{-2}$. Needle-like voids initiated at the cathode/solder interface as a result of the outward diffusion of Zn atoms of the Zn-rich phase (Kuo and Lin, 2008).

## 9.4 Formation of whisker and hillock

The formation of Sn whisker in electronics is well recognized in the electronic packaging industry and occurs on the contingent of having adequate compressive stress (Tu, 1994). There are various sources of compressive stress, such as the interaction between Cu and Sn in a thin film. The reaction forms IMC that causes compressive stress because of volume change. The formation of whisker relieves the stress; Sn atoms sprout out from the crack of the surface oxide layer and thus grow as whisker (Chen *et al.*, 2010, Tu, 1994).

As being a result of the compressive stress, both hillock and whisker are formed owing to the extrusion of Sn atoms and may be found in a same specimen. It is possible to distinguish between whisker and hillock by the difference in aspect ratio: whisker is defined as having an aspect ratio of greater than five, whereas that for hillock is less than two (Guo, 2009). Electromigration accelerates the diffusion of atoms within the matrix. The accumulation of atoms may give rise to compressive stress within the solder, either around electrodes, or at the solder/IMC interface. Electromigration thus serves as the direct driving force for building up compressive stress.

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Although mass accumulation is of importance in the build up of stress, an *in situ* study with synchrotron X-ray microdiffraction showed that stress may also build up within a Sn0.7Cu flip chip solder joint owing to anisotropic diffusion of Sn (Chen *et al.*, 2009). Sn crystal is body-centered tetragonal with quite different diffusivity in different lattice directions. The self-diffusivity of Sn in the *a*-direction is twice that in the *c*-direction (Dyson, 1967). Current stressing across the solder bump at $1.25 \times 10^4$ A cm$^{-2}$ at 70 °C gradually builds up a compressive stress within the grain at the current crowding end (Chen *et al.*, 2009). Electromigration of atoms in the solder matrix may be retarded by the existing stiff phase. The stiff structure does not migrate during current stressing. The migrating atoms accumulate at the interface between the solder matrix and the stiff structure. Portions of the Sn migration in a Sn9Zn solder under a current density of $10^5$ A cm$^{-2}$ at 80–140 °C was stopped in front of the Zn rich phase. The Sn accumulated at the interface between solder and Zn precipitate builds up compressive stress which extrudes Sn to form Sn whisker or hillock. The growth of Sn whisker was also enhanced by the current stressing temperature (Chen *et al.*, 2009).

In a Cu/Sn3.5Ag/Au solder structure, $AuSn_4$ IMC formed in the matrix after reflow. The IMC was seen to rotate after current stressing with a current density of $2.56 \times 10^3$ A cm$^{-2}$ at 100 °C. Mechanical stress thus induced by IMC rotation may also be the major driving force for whisker and hillock formation (Chiu and Lin, 2009). On the other hand, the growth of whisker or hillock may be retarded by the IMC formed in the solder. The formation of larger amounts of IMC at higher temperatures in the Sn0.7Cu solder bump blocks the migration of Sn. Consequently, the growth of whisker or hillock at the anode is hindered owing to the diffusion barrier effect of the IMC in the solder matrix (Liang *et al.*, 2010). The formation of Sn whisker is usually regarded as a deficit for reliability concern. However, it was reported that a solder bump with under-fill protection was not able to form whisker to relieve the stress inside the bump. Such circumstances result in the buildup of stress at anode and thus cracking (Lee *et al.*, 2001).

## 9.5 Grain reorientation and grain rotation

The resistance of a Sn stripe was found to decrease exponentially with time when stressed with a current of $6.25 \times 10^4$ A cm$^{-2}$ at 150 °C (Lloyd, 2003). The decay in resistance was attributed to the reorientation of the grain structure. The anisotropic behavior of Sn crystal exhibits an electrical resistivity difference by more than 40% at 0 °C between the *a*-direction and *c*-direction of the body-centered tetragonal Sn crystal (Burckbuchler and Reynolds, 1968). The reorientation aligns the direction of low resistance of the Sn crystal in the direction of electromigration, thus reducing the electromigration-

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induced chemical potential (Lloyd, 2003). The results of synchrotron X-ray microdiffraction investigations grain by grain show the change in grain orientation. It indicates that the grain with low resistance grows whereas that of high resistance gradually shrinks. The grain growth therefore occurs at the expense of the high-resistance grains. This behavior was ascribed to electromigration rather than Joule heating effect (Wu *et al.*, 2004).

The behavior of grain reorientation to reduce resistance, to a more macroscopic view, also appears to cause rotation of the grains. Grain rotation occurs in a Sn stripe after current stressing with a current density of $2 \times 10^4$ A cm$^{-2}$ at 100 °C for 500 h. The rotation of a piece of grain needs a torque, which is thought to mainly come from the different direction of the vacancy flux driven by electromigraion (Wu *et al.*, 2005). The diffusion of vacancy and atoms along the grain boundary is different for neighboring grains with different orientations. The vacancy becomes supersaturated at the anodic-side grain boundary and undersaturated at the cathodic-side grain boundary. The divergence in vacancy flux builds up a stress in the grain which serves as the origin of the torque (Wu *et al.*, 2005). A theoretical expression indicates that the rotation speed, the angular velocity, of the grain is enhanced, thus affecting current and temperature. A higher current density produces a larger electron wind force, which drives larger atomic flux to the anode and a larger vacancy flux to the cathode. A larger vacancy flux divergence is thus produced to generate greater torque (Wu and Hsieh, 2008). An electrically isotropic material does not exhibit vacancy flux divergence and thus the grain rotation was not observed for Al and Cu. The grain rotation behavior was also observed for the $AuSn_4$ IMC formed in a Cu/Sn3.5Ag/Au solder structure after current stressing with a current density of $2.56 \times 10^3$ A cm$^{-2}$ at 100 °C. The $AuSn_4$ IMC formed and grew rapidly. The large IMC within the joint essentially blocks the atom diffusion. Accumulation of Sn in front of the IMC induces the formation of both whisker and hillock (Chiu and Lin, 2009).

## 9.6 Dissolution and recrystallization

Current stressing through the solder joint encounters different metal structures including metallization and solder. The thin metallization at the electrode side, especially the cathode, may induce Joule heating because of its high resistance. The Joule heating induces dissolution of the metallization layer. In a μBGA solder joint the thin Cu trace on the component side encounters a higher current density and thus higher temperature rise than the solder joint. On the opposite side, the Cu trace on the board, larger in area and thicker, shows a lower temperature rise. A greater dissolution rate of the Cu trace on the component side is associated with the melting of the 63Sn37Pb solder joint when stressed at high current density (Alam *et al.*,

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2006, Wu and Chan, 2005). In such a case, dissolution of Cu trace on the anodic board side was observed owing to melting of the solder joint even though the current density on the board side is lower. When the solder joint remains in the solid state, the anodic copper trace dissolves and migrates to the anode (Tu *et al.*, 2000, Hu *et al.*, 2003). $Cu_6Sn_5$ IMC was formed on the anodic board side even though there is an electroless Ni–P metallization layer (Alam *et al.*, 2006). The polarity behavior between the cathode and the anode side gives rise to thicker $Cu_6Sn_5$ and $Cu_3Sn$ IMC at the anode side than the cathode side, apparently owing to the dissolution of the Cu trace at the cathode side. Electromigration accelerates the dissolution of Ni and Cu of a BGA joint with Ni(P)/SnPb/Ni(P) structure when stressed with a current density of $3.0 \times 10^3$ A cm$^{-2}$ at 120 °C. The fast dissolution enhances both the formation of $(Cu,Ni)_6Sn_5$ at the current crowding region and $Ni_3Sn_4$ at the anode side (Lu *et al.*, 2009b). $Cu_6(Sn,In)_5$ compound formed in a Sn3Ag3Bi10In solder stripe after current stressing as a result of the dissolution of Cu into the solder to react with In and Sn. The Cu dissolution from the cathode resulted from the current stressing (Wu and Sun, 2009). Cu and Ni may dissolve rapidly in solder along the orientation of Sn grain (Lu *et al.*, 2008). Both Cu and Ni exhibit several orders of faster diffusion along the *c*-axis than either the *a*- or the *b*-axis of Sn crystals (Dyson *et al.*, 1967, Yeh and Huntington, 1984). It is reasonable to imagine that the synergism of electric current stressing and grain orientation will induce extreme fast dissolution of the metallization UBM into the solder. A dissolution flux of $9.98 \times 10^{10}$ atoms cm$^{-2}$ s$^{-1}$ was calculated for Cu under electromigration through a Cu/Sn/Cu solder joint at a constant current density of $5.3 \times 10^3$ A cm$^{-2}$ (Tseng *et al.*, 2010). The flux tends to be larger at the current crowing region.

The electromigration-induced dissolution behavior not only occurs to the thin metallization layer of a solder joint but also to the IMC formed after reflow in the solder joint. A flip chip solder, 63Sn37Pb, joint with Cu/Ni(V)/Al UBM on the chip side and Au(30 nm)/Ni(10 μm) on the Cu trace of the FR4 substrate, was investigated with current stressing. The electromigration study was conducted at 100–140 °C with a current density of $1.90–2.75 \times 10^4$ A cm$^{-2}$. The Cu–Sn IMC at the cathode UBM side dissolved after current stressing with $2.25 \times 10^4$ A cm$^{-2}$ at 125 °C. The dissolution of IMC reveals the underneath diffusion barrier Ni(V) layer followed by the exposure of Al layer (Choi *et al.*, 2003). This dissolution behavior thus raises a concern about the reliability of the solder bump. The dissolution of IMC also occurs in the Sn3Ag3Bi10In solder system. $Cu_6(Sn,In)_5$ IMC and the ζ phase in the cathode region, formed after reflow of the Cu/solder/Cu joint in a Si U-groove, dissolve after current stressing at a current density of $1 \times 10^3$ A cm$^{-2}$ at 150 °C for 120 h (Wu and Sun, 2009). $Cu_6(Sn,In)_5$ IMC and the ζ phase grew to less than half of the dimension with thermal aging at a

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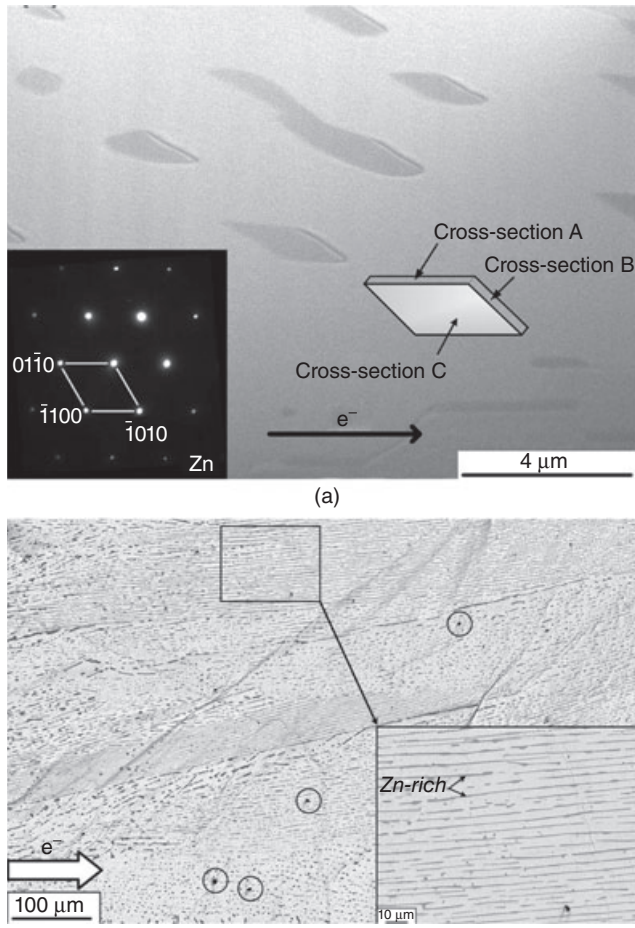
higher temperature, 180 °C, for the same time duration. The occurrence of dissolution in the cathode area leads to atom flux toward the anode. The ζ phase in the solder matrix and the anode region grew during current stressing when encountering the atomic flux supplied by the dissolution. In view of the fact that the ζ phase is a thermodynamically stable phase, the disappearance of it at the cathode side was thought to be caused by the electron current from the cathode.




*9.4* (a) The recrystallized Zn nanosheet grains in a Sn9Zn solder after current stressing, (b) morphology of the edge of the nanosheet grains at the lower magnification shows alignment of Zn-rich grains along the direction of the election flow after electromigration for 230 hours (Kuo and Lin, 2009).

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Electric current can refine the microstructure of a metal alloy. The effect was ascribed to the enhancement of the nucleation rate (Conrad, 2000). For the situation of deformed metallic specimen, the high current density at the deformed area causes nucleation by the pinch effect. Recrystallization occurs for a electric current pulse that provides an instantaneous high energy input that causes a high local temperature increase (Conrad, 2000, Song and Wang, 2008). Recrystallization also occurs in a current stressed Sn–9Zn solder joint. The stabilized equiaxial Zn-rich phase of the eutectic Sn-9Zn solder wire, 4.8 mm length with 1.2 mm diameter, gradually disappears when stressed with $2.6 \times 10^3$ A cm$^2$ at 100 °C. The equiaxial crystals transform into a two-dimensional sheet structure of 200 nm thick of which the layer lattice stacks in the [0001] direction, compared with the [2000] and Zn[10$\bar{1}$0] textures of the stabilized equiaxial grains, Fig. 9.4 (Kuo and Lin, 2009). The driving force for the recrystallization behavior was not discussed in detail therein. The same group recently conducted a series studies on another solder. The *in situ* SEM results indicate an excess dissolution of the second-phase precipitates during electromigration. It is believed that the recrystallization results from the supersaturation which drives recrystallization. Nevertheless, the refinement as a result of the recrystallization seems to induce a high-energy state in the system. The mechanism of this recrystallization behavior still remains to be explored.

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# 10

# Electromigration in flip-chip solder joints

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**Abstract**: This review is devoted to four types of physical failure mechanisms in microelectronic devices for high-current density applications; those failures are electromigration (EM), Joule heating-induced failures, stress-related damage, and thermomigration (TM). In practice, some of these failure mechanisms occur together so that the real root cause cannot easily be detected and understood. Reliability designers need to be well informed to evaluate the electrical characteristics, thermal characteristics and mechanical strength for solder interconnects in advance. Recent progress in failure mechanism evaluation is summarized and a critical overview of the basis of atomic transport, diffusion kinetics, morphological evolution, and numerical simulation is presented. Special emphasis is on the understanding of EM interactions with other failure mechanisms. In addition to this review of the current knowledge, the remaining challenges as well as future directions are also discussed.

**Key words**: solder, electromigration, Joule heating, stress, thermomigration, interconnects.

## 10.1 Introduction

### 10.1.1 Solder interconnects for advanced electronic packaging

With the trend towards higher integration and further miniaturization of Si-based devices, electronic packaging is successively requiring a higher input/output (I/O) density, smaller feature size, and better performance. Concurrently, the flip-chip solder interconnect has established its leadership role for high current density packages, as thousands of solder bumps are fabricated onto one single chip. To meet an even higher demand for device performance, the I/O number is expected to increase, whereas the dimensions of each individual bump will accordingly need to shrink.

According to the 2003 International Technology Roadmap for Semiconductors (ITRS), a significant downsizing in flip-chip packaging is anticipated.[1] Figure 10.1 shows the anticipated variation in pad diameter, pad pitch and line width. In addition, the bump size is expected to reduce



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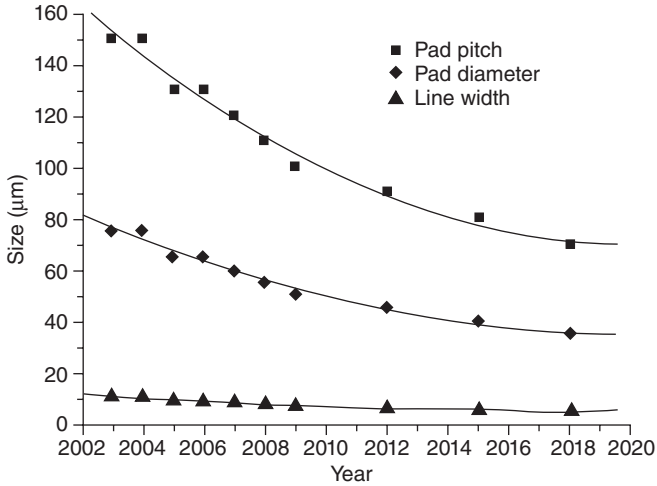


*10.1* A downsizing in flip-chip packaging, based on 2003 ITRS edition.[1]

along with the pad size and pitch. At present, the diameter of a solder bump in use is about 100 μm or less.[2] In 2007, the diameter of micro-bumps had been decreased to 20 μm.[3] This persistent scaling-down inevitably places severe challenges on the reliability of micro-devices, as discussed later.

## 10.1.2 Challenges of high current density applications

At present, in the microelectronic industry, each solder joint is designed to carry 0.2 A, and the current will be doubled in the near future.[2] Therefore, the average current density through a 50 μm diameter solder joint may approach $10^4$ A $cm^{-2}$. This demands a reduced cross-section of the conductive lines and solder interconnects, in spite of the fact that these structures are expected to conduct such a high current density. Meanwhile, because Joule heating is proportional to the square of the current density, the local temperature of conductive lines and solder bumps rises substantially. Also, during field service, the solder joints experience a temperature rise of at least 100 °C, to approximately 82 and 76% of the melting temperatures of eutectic SnPb and SnAgCu, respectively. As a consequence, under the combined effect of a high current density and a high homologous temperature, efficient diffusion of atoms in the lattice is anticipated.[4] This renders electromigration (EM) a serious reliability issue in the application of high current density packages.

EM is defined as a diffusion-controlled mass transport phenomenon owing to the application of electrical current. In 1961, Huntington and Grone proposed that a thermally activated metal ion becomes essentially

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free in the lattice and is acted upon by two opposing forces (a direct force and an electron wind force) in a metal.[5] Also, Huntington and Grone identified the electron wind force as the primary driving force responsible for the EM failure observed in interconnects. The electron wind force is further explained as one force experienced by a metal ion in the direction of the electron flow owing to the momentum exchange between the moving electrons and the ion. Therefore, the phenomenological equation for the atomic flux due to EM ($J_{em}$) is described as:

$$J_{em} = Cv = C\frac{DF}{kT} = C\frac{D}{kT}Z^*eE = C\frac{D}{kT}Z^*e\rho j, \qquad [10.1]$$

where $Z^*$ is a dimensionless quantity known as the effective charge or the effective valence that reflects the direction and magnitude of the momentum exchange, $e$ is the electron charge, $E$ is the electric field, $\rho$ is the resistivity, $j$ is the current density, $C$ is the concentration of diffusing atoms, $v$ is the drift velocity of these atoms, $D$ is the thermally-activated diffusivity, and $kT$ is the average thermal energy.

Regarding the EM of tin and lead in solder alloys, Brandenburg and Yeh first published research in 1998.[6] EM causes the net atom transport of solder material along the direction of the electron flow. Since 2002, ITRS has started to include this reliability problem for industrial attention.[7] Table 10.1 lists the near-term reliability challenges requiring concern in current assembly and packaging techniques.[3] According to the 2007 ITRS, EM becomes a more limiting factor of high current density packages, such as wafer-level packaging (WLP) for micro-electro-mechanical systems (MEMS). It is suggested that physical failure mechanisms such as EM, and thermal migration in combination with mechanical stresses, should be understood and modeled for practical life assessment. In particular, solder and the under bump metallurgy (UBM) need to be well designed to support a high current density and minimize or avoid EM.

Also, thermal dissipation is addressed as a critical factor of reliability considering the large Joule heating generated by the on-chip metal

*Table 10.1* Assembly and packaging – difficult challenges[3]

| Difficult challenges | Summary of issues |
|---|---|
| High current density packages | Electromigration becomes a more limiting factor. It must be addressed through changes in materials together with thermal/mechanical reliability modeling<br>Whisker growth<br>Thermal dissipation |

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interconnects. One should appreciate that the cross-sectional area of conductive lines on the chip has been decreased significantly with the trend towards miniaturization, as shown in Fig. 10.1. It is true to say that the on-chip interconnects used in electronic packages may be based on Al or Cu materials. However, most concern is with interconnects based on Al, where Joule heating is more pronounced (the resistivity of Cu is about 60% of that of Al). For a flip-chip interconnect, the electrical resistance of the Al traces is at least one order of magnitude higher than that of the solder joints and Cu conductors, and thus the Al traces are the primary heat source. A significant Joule heating will accelerate the EM process in the neighboring solder joints, but also result in the degradation of UBM layers and even the Al trace itself.

Another concern is the formation of compression and tension regions inside a solder joint, when atoms are driven from the cathode to the anode by the electron wind force. Stress generation and relaxation are issues under exploration, and stress-related damage under a current density should be paid considerable attention. In addition, mechanical properties are direct indicators of strength and long-term durability. It is understandable that EM would exert a certain effect on the mechanical transition of solder interconnects. As an important reliability factor, the mechanical behavior of solder interconnects for high current density applications also needs to be carefully considered.

Moreover, owing to the significant heat accumulation, the atomic migration process, thermomigration (TM), may be triggered and influence the reliability of packages. Owing to differences in electrical resistance and thermal dissipation of individual parts within the flip-chip interconnect structure, it is predicted that the heat accumulated at the chip side will be larger than that at the substrate side. This variation inevitably leads to a considerable temperature gradient across solder joints, which can provide a driving force for atomic diffusion to trigger TM. More exactly, the driving force of TM comes from both the energy transported by the moving atoms and the interactions with the usual heat carriers in the lattice.[8] The phenomenological equation for the atomic flux owing to TM ($J_{tm}$) is:[9]

$$J_{tm} = Cv = C\frac{DF}{kT} = C\frac{DQ^*/N}{kT^2}(-\Delta T) \qquad [10.2]$$

where $Q^*$ is the heat of transport and is the heat flow per mole that must be supplied to maintain unit molar flow in the steady state, $N$ is Avogadro's number, and $\Delta T$ is the thermal gradient. The other terms in the above equation have been defined under equation [10.1]. Being a potential reliability concern for flip-chip solder interconnects, TM induced-void or pore formation has also been introduced in the 2007 ITRS.[3]

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### 10.1.3 Scope of this review

During field service, all the factors discussed are supposed to combine and act concurrently, thus further complicating the failure processes. Therefore, a quantitative understanding of the physics and mechanics of each failure mechanism strengthens the design and life prediction in flip-chip solder interconnects, which is of particular interest to both those in industry and in academia.

Four types of failure mechanism are presented in this review. Section 10.2 addresses the void formation during EM in solder interconnects. In addtion, from an engineering standpoint, this section summarizes the lifetime statistics and reliability evaluation of EM of solders. Section 10.3 reviews the dissolution of the UBM owing to an accelerated interstitial diffusion, and the diffusion of on-chip Al trace under Joule heating, then introduces research results on the time-dependent melting behavior of solder interconnects under current stressing. A summary of stress-related degradation in solder interconnects is presented in section 10.4. The morphological evolution owing to EM and the back stress induced are described. Also some mechanical deformation and degradation mechanisms under current stressing are summarized as a part of an overall understanding of the mechanical behavior. Section 10.5 discusses the reliability concerns of TM. The thermotransports of Pb, Sn, Cu and Bi in solder interconnects under a thermal gradient are introduced. Lastly, but importantly, issues that need to be investigated in the near future are proposed in section 10.6.

## 10.2 Electromigration (EM)-induced voiding failure of solder interconnects

### 10.2.1 Nucleation and growth of voids at the interface

During EM, atomic diffusion-induced microstructural evolution includes not only phase separation[6,10–16] and phase coarsening,[17–20] but also void creation at interfaces. Figure 10.2 displays the progress of void growth in Sn3.5Ag1.0Cu solder joints under a current density of $1.5 \times 10^4$ A cm$^{-2}$ at 125 °C.[14] Figure 10.2a shows the typical morphology of the interface before the experiment. After a stressing time of 75 h, as shown in Fig. 10.2b, voids were initiated from the upper-right corner, and gradually displaced the current to the surrounding areas, resulting in a lateral growth. Because the growth of voids induced the redistribution of the current, it is also reasonable to find that the voids were developed towards the periphery of the UBM opening, where the original current density was low. This experimental finding verifies the finite element simulation by Liang *et al.*[21] Figure 10.2c shows the microstructural development after 280 h. It is

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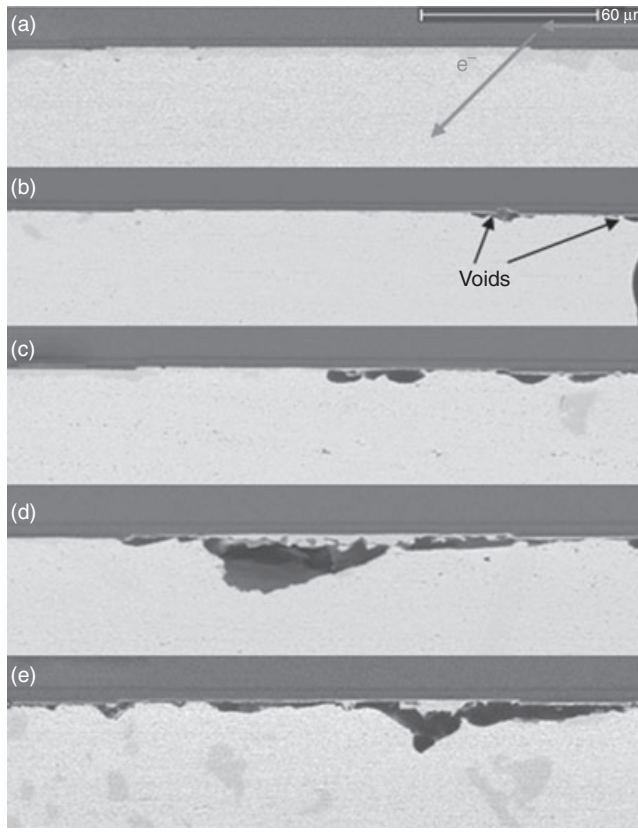


*10.2* SEM images of the morphological evolution in Sn3.5Ag1.0Cu solder joints under a current density of $1.5 \times 10^4$ A cm$^{-2}$ at 125 °C (a) before the experiment, time point A, (b) after 75 h, 14% of the failure time, time point B, (c) after 280 h, 53% of the failure time, time point C, (d) after 425 h, 81% of the failure time, time point D, and (e) after 515 h, 98% of the failure time, time point E.[14]

evident that the voids continuously extended from the right-hand to the left-hand regions. Figure 10.2d displays further void growth after 425 h. The propagation of voids decreased the effective contact area of the current path and induced a more serious current crowding, and thus accelerated the void growth along the interface. This process continued until the voids finally spread across the complete contact window at 515 h, as shown in Fig. 10.2e.

From Figure 10.2, it is believed that the first void nucleation took less than 14% of the failure time. The failure time was then more dependent on the void growth than the void nucleation. Likewise, Chiu and Chen moni-

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tored void formation and propagation in Sn37Pb solder joints under a current density of $6.5 \times 10^3$ A cm$^{-2}$ at 150 °C.[22] They found that voids started to form at approximately 10% of the failure time and grew for the remaining 90% of the failure time. The voiding behavior is different from the EM behavior of Al and Cu interconnects. In Al and Cu interconnects, failure is basically controlled by the nucleation of voids, and growth becomes very rapid once the voids are produced. By contrast, Yeh *et al.* proposed that it took 88% of the failure time to initiate the first few voids, whereas only 12% of the failure time was spent in void propagation until the final open failure.[23] According to the study by Yeh *et al.* the incubation time for void nucleation was relatively long.

Based on the results from the time points A to E in Fig. 10.2, the growth rate was found to be about 0.32 μm h$^{-1}$ for the whole process, which matches well with the result by Chiu and Chen.[22] Chiu and Chen found a void growth rate of 0.3 μm h$^{-1}$ in the later stages in Sn37Pb solder joints. However, this is different from the investigation conducted by Zhang *et al.*[24] Zhang *et al.* reported a void growth rate of 4.4 μm h$^{-1}$ in Sn4.0Ag0.5Cu solder joints that experienced EM under a current density of $3.7 \times 10^3$ A cm$^{-2}$ at 146 °C. A theoretical value was also calculated under a continuity condition according to the kinetic model Zhang *et al.* proposed, which was in accord with the experimental result. However, similar to research in Al interconnects, thin-film test structures should be prepared to directly measure the material depletion in solder over an EM period, so that the atomic drift velocity may be precisely obtained. This method has been utilized to explore EM parameters in Sn3.5Ag solder.[25]

The growth of voids has been understood in relation to a variation in electrical resistance. A Kelvin structure was designed and employed to monitor the resistance variation of a solder joint with the propagation of voids.[26,27] A change in bump resistance as small as 0.01 mΩ could be detected using the Kelvin structure, and it was effective for monitoring how the void growth induced the resistance change in a single solder joint. It was found that, when the percentage depletions of the contact opening were about 50 and 80%, the maximum resistance increases could reach 70% and 250% of its initial value, respectively. Three-dimensional (3D) simulations for different stages of void propagation by Liang *et al.* also fit well within these results.[21]

Figure 10.3 shows the typical variation in voltage as a function of time. Solder interconnects experiencing EM mostly exhibit such a characteristic of the variation in resistance.[23,28,29] There is a long incubation time with very little resistance change below 90% of the stressing time. The solder joints only contribute to a minor resistance in the whole interconnect structure as compared with the Al traces and the Cu conductors; thus, the effect of void propagation on the resistance of the interconnect structure was less

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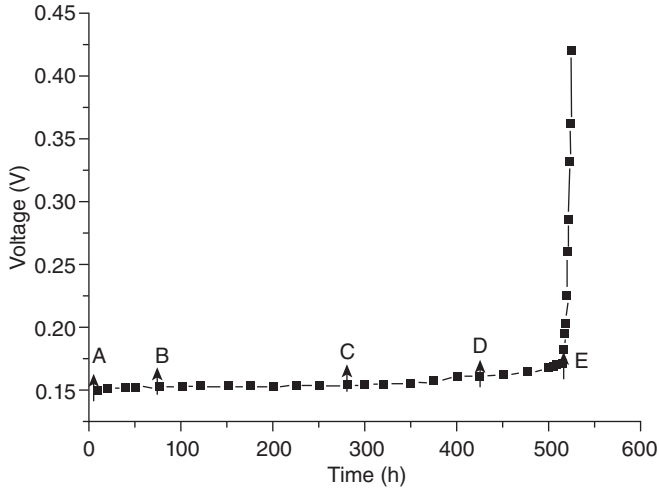


*10.3* Voltage as a function of time when an interconnect structure was stressed by 1.2 A at 125 °C (Note that this data arises from the same experiments as in Fig. 10.2, and the time points A to E refer to the same time points.[14]

significant before the UBM was completely detached from the solder. This is why solder interconnects mostly retained a low electrical resistance in the early stages of the stressing time, although void accumulation has occurred in the solder joints. After the UBM was completely detached from the solder, the resistance rose abruptly to an open circuit.

## 10.2.2 Lifetime statistics and the reliability of EM

From an engineering standpoint, a mean-time-to-failure (MTTF) estimation of solder interconnects is of great interest, and a systematic reliability evaluation of EM is needed. For Al interconnects, it is reported that the EM lifetime mostly follows a log–normal distribution. Black's model was introduced to describe the EM lifetime of a solder based on the assumption that the failure is controlled by void damage, and a log–normal function has been applied frequently.[29–31] However, the reason for such a log–normal distribution has not been clarified. However, a Weibull analysis has been performed on time-to-failure (TTF) data in other studies.[6,32] In our case, the EM failure of Sn3.5Ag1.0Cu solder joints followed Weibull statistics closely, with current densities ranging from $1 \times 10^4$ to $2 \times 10^4$ A cm$^{-2}$ at 100, 125, and 150 °C.[14] Figure 10.4 illustrates the distribution function under various current densities at 125 °C. As expected, the reliability of EM degraded with an increase of current density.

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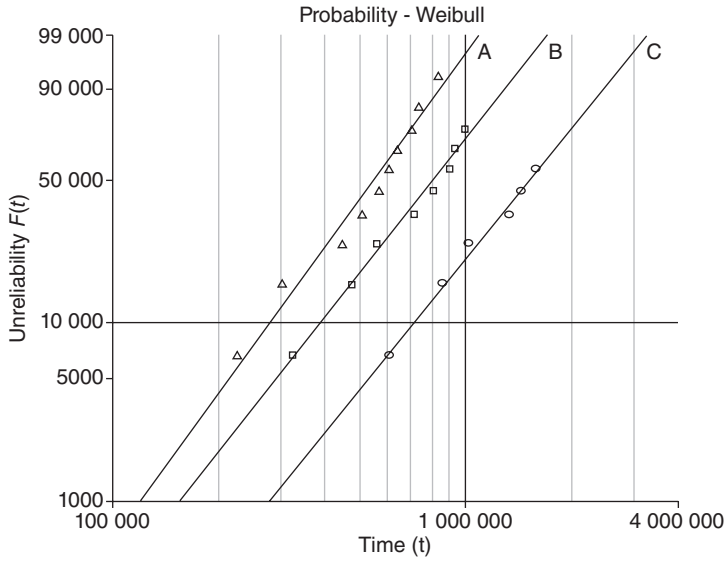


*10.4* Weibull cumulative distribution under various current densities at 125 °C (A: $2.0 \times 10^4$ A cm$^{-2}$; B: $1.5 \times 10^4$ A cm$^{-2}$; and C: $1.0 \times 10^{-4}$ A cm$^{-2}$).[14]

Nevertheless, the predicted lifetimes did not match well with the measured ones, particularly under a higher current density.[33] As a result, this study suggests that the model should be modified to include the effect of current crowding and Joule heating. A modified Black's equation was proposed by inserting a multiplying factor ($c$) of the current density and a temperature increment ($\Delta T$) into Black's equation:[33,34]

$$\mathrm{MTTF} = A\frac{1}{(cj)^{\mathrm{m}}}\exp\left[\frac{Q}{k(T+\Delta T)}\right] \qquad [10.3]$$

where $A$ is a constant, $j$ is the current density in the solder, $m$ is an exponent for current density, $Q$ is the activation energy for EM, $k$ is Boltzmann's constant, and $T$ is the average temperature.

By adding the current factor and a constant temperature increment, Choi *et al.* obtained activation energies of 0.5 and 0.8 eV for SnPb and SnAgCu solders, respectively.[33] Chae *et al.* also considered the effect of Joule heating: the activation energy calculated was 0.86~0.94 eV and the current density exponent was 2.1~2.2 for SnAg solder joints.[29] In addition, by virtue of a numerical simulation and temperature coefficient resistance method (TCR = $\Delta R/R_0\Delta T$, $R_0$ is the resistance of the Al trace at $T_0$, $\Delta R$ is the resistance variation, and $\Delta T$ is the temperature rise), we deduced the $c$ and the $\Delta T$ (depending on the applied current and ambient temperature), respectively.

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*Table 10.2* Statistics of EM reliability parameters of lead-free solders[14,29,33,34]

| Research group | Test conditions $T$ (°C), $j$ (A cm$^{-2}$) | Activation energy $Q$ (eV) | Current density exponent $m$ |
|---|---|---|---|
| Univ. of Texas at Austin (Sn3.5Ag)[29] | 115~150, 4.12~5.67 × 10$^4$ | 0.86~0.94 | 2.1~2.2 |
| Univ. of California, LA (SnAgCu)[33] | 125~160, 2.75~3 × 10$^4$ | 0.8 | – |
| National Tsing Hua Univ. (Sn3Ag0.5Cu)[34] | 125~165, 0.74~1.68 × 10$^4$ | 0.88 | 2.11 |
| EPA, City Univ. of HK (Sn3.5Ag1.0Cu)[14] | 100~150, 1.0~2.0 × 10$^4$ | 0.58~0.66 | 1.46~1.89 |

The average activation energy obtained was about 0.62 eV, and the current density exponent ranged from 1.46 to 1.89.[14] Table 10.2 presents the EM reliability parameters for Sn-based lead-free solder interconnects from accelerated life tests in different studies.[14,29,33,34]

More recently, Chiang *et al.* compared the predicted values based on Black's equation, with the predicted values based on the modified equation, and the measured MTTFs under test conditions of different current densities and temperatures. They found that the deviation of predicted values from the experimental results were reduced based on the modified equation.[34] Indeed, further effort is necessary to identify the actual current density and bump temperature in solder interconnects. Also, the physics of failure after accelerated life tests needs to be established to confirm its consistency with the proposed failure mechanism. Otherwise, the EM reliability would be incorrectly evaluated.

## 10.3 Joule heating-enhanced dissolution of under bump metallurgy (UBM) and the diffusion of on-chip metal interconnects

### 10.3.1 Effect of Joule heating owing to current stressing

In high-current density packages, heat accumulation cannot be ignored because Joule heating is proportional to the square of the current density. The current-crowding effect inevitably leads to a local temperature rise, which in turn accelerates the nucleation and growth of voids inside the solder joint. More significantly, as the foremost heat source, Joule heating from the on-chip metal interconnects is of particular concern. This was verified with thermal infrared measurements.[35] Figure 10.5 shows the temperature distribution in a flip-chip interconnect when stressed by $10^4$ A cm$^{-2}$ at an ambient temperature of 70 °C. The temperature in the middle of the Al

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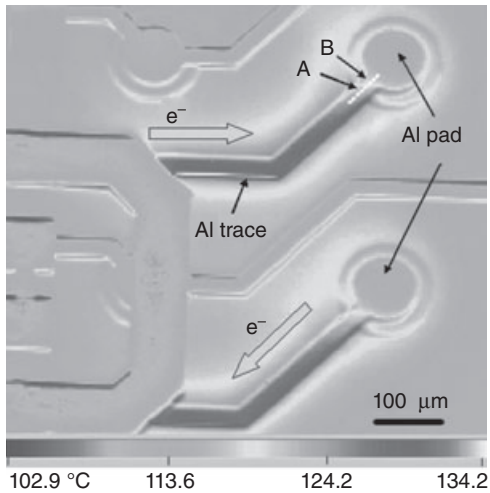


*10.5* Thermal infrared measurement for the chip side, with the Al trace exhibiting the highest temperature.[35]

traces was much higher than that at the circular Al pads. The edges of the UBM (marked point A) and the passivation openings (marked point B) also exhibited higher temperatures than the Al pads above the solder joints. Numerical simulation of the temperature distribution within solder interconnects supported the infrared measurement.[35–37]

Since the Al trace is the dominant heat source together with local Joule heating inside of the solder, it is expected that hot spots should occur where the Al traces enter the solder joint. Near this hot spot region, atomic diffusion is thermally accelerated so that the UBM layer is damaged. Also, lattice diffusion of Al atoms is possibly initiated because of the local high-current density itself. These mechanisms may be combined and this is discussed later.

## 10.3.2 Dissolution of UBM layers and possible solutions

The dissolution of a Cu UBM in a eutectic Sn37Pb solder joint under current stressing has been detected.[38,39] Under a current density of $10^3$ A cm$^{-2}$ at 150 °C for 0.5 h, the solder joint failed with an open circuit, as one of the corners of the Cu UBM was dissolved and replaced by solder according to the microstructural analysis. Hu and coworkers also reported the rapid, asymmetrical, and localized dissolution of a Cu UBM at the cathode side.[40,41] The average dissolution rate was 1 μm min$^{-1}$ when the current density through the eutectic Sn37Pb solder joint was $2.5 \times 10^4$ A cm$^{-2}$ at 100 °C. From the location and geometry of the dissolved Cu, the research suggests

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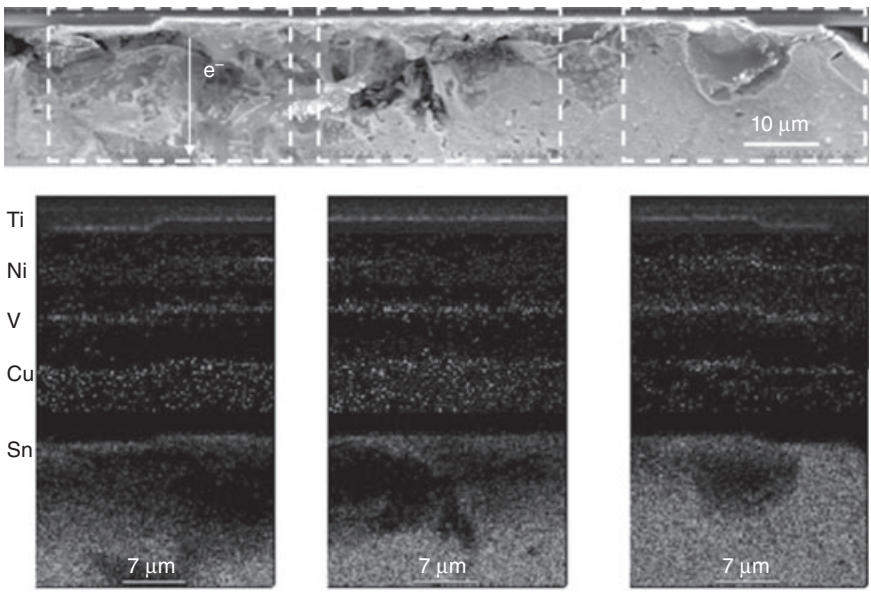
that current crowding played a critical role in this rapid dissolution. When the current density was increased to $4 \times 10^4$ A cm$^{-2}$, extensive dissolution of the Cu UBM occurred even at an ambient temperature of 30 °C.

The rapid dissolution of Cu UBM is attributed to an interstitial diffusion of noble and near-noble metals enhanced by Joule heating. It is well known that the interstitial diffusion of dilute elements in tin is significant.[42–44] A series of fundamental studies on diffusion and EM of Cu, Ni, Ag and Au in lead–tin alloys have been developed since the 1980s.[45–47] As the lattice constants of *a* and *b* in tin are much larger than that of the *c* axis, the open structure along the *c* axis facilitates faster interstitial diffusion than along the other orthogonal directions. Taking Ni for example, the diffusivity of Ni along the tetragonal *c* axis is about $7 \times 10^4$ times than that at right angles at 120 °C,[44] and the EM is very fast, relatively.

Therefore, it is not difficult to understand why Ni was consumed during EM experiments also, although Ni is used as a diffusion barrier in UBM application. Figure 10.6 illustrates the effect of EM on a multilayer UBM film of Ti (0.2–0.5 μm) / Ni(V) (0.325 μm) / Cu (0.5–1.0 μm).[48] It was found that, after experiencing a downward electron flow, the Ni and Cu constituents in the UBM began to spread into the solder, and the UBM was gradually consumed. In this instance, voids formed at the UBM/intermetallic




*10.6* Elemental mapping at the UBM/IMC interface in a Sn3Ag1.5Cu solder joint after 1967 h under a current density of $1 \times 10^4$ A cm$^{-2}$ at 150 °C.[48]

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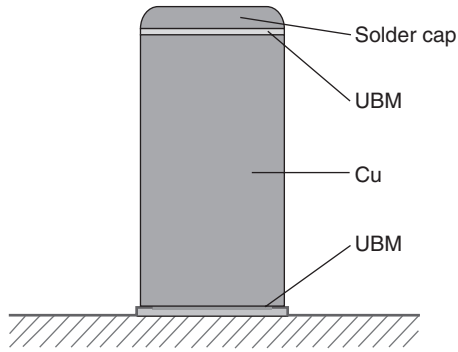
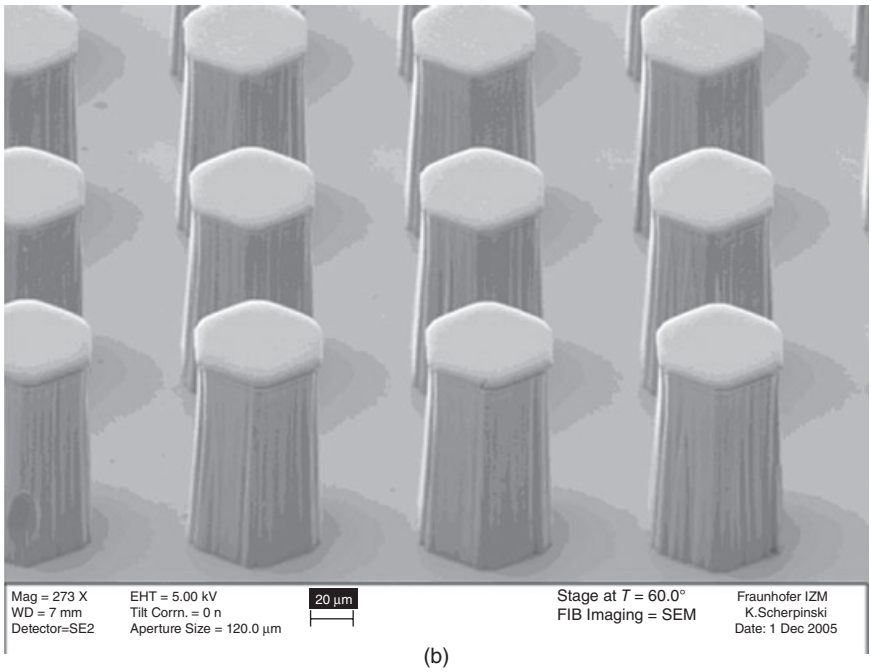
compound (IMC) interface owing to UBM consumption under the combined effect of interstitial diffusion and large Joule heating.

It has been proposed that a possible solution to the effects of EM in solder joints would be a thick Cu pillar. The thick Cu pillar could be fabricated as the UBM, and a thin cap layer of solder would be required for the bump, as shown in Fig. 10.7.[3] An additional electroplated Ni layer has been




(a)




(b)

*10.7* (a) Schematic diagram of a Cu pillar bump with a solder cap, and (b) focused ion beam (FIB) image of Cu pillar bumps with a height of 80 μm.[3]

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suggested to suppress Cu diffusion into the solder body, thus practically inhibiting IMC formation and Kirkendall voiding.[49] It is expected that this will be effective in dealing with the problem of UBM dissolution and void accumulation, because the thick Cu pillar is designed to spread the current from the contact to an approximately uniform and low density. This proposal has been supported by experimental studies and numerical simulation.[50,51] However, a substantial formation of IMC at the interface is becoming an issue. Also, TM may be initiated because a large temperature gradient is generated across the shallow solder interconnects.

Recent studies have noted that the rotation of β-Sn grains occurred in Sn-based solder under current stressing because of their anisotropic properties.[52,53] This re-orientation resulted in a realignment of Sn grains along with the current flow, thereby reducing the resistance of the solder. It is also known that the diffusion of Ni/Cu in UBM was much enhanced along the *c* axis of Sn crystals, which contributed to the dramatic dissolution of the UBM. Therefore, one should argue that the orientation of Sn grains is closely related to the reliability of Sn-base lead-free solders. Lu *et al.* investigated the effect of Ag in a Sn-based solder and concluded that the grain re-orientation of Sn was blocked owing to the presence of cyclic twinning and a stable $Ag_3Sn$ IMC network; in turn, the dissolution of UBM was comparatively mitigated.[54] Lu *et al.* further explored the effect of an additional 0.6 wt% Zn in Sn1.0Ag solder and obtained a positive result.[55] The Zn doping stabilized the $Ag_3Sn$ and $Cu_6Sn_5$ IMC networks, and suppressed the formation of $Cu_3Sn$ IMC. More importantly, polycrystalline-like structures formed at the solder/UBM interface. Although it seems that Zn doping could not control the grain orientation in bulk solder, the strong binding with Cu effectively slowed down the Cu diffusion, and thus stabilized the solder microstructure. Lu *et al.* present a creative study that explores the doping effect on the microstructural evolution and thus the enhancement of EM resistance. Further nano-doping of solder is also anticipated to support a higher current density and to attenuate the EM damage.

### 10.3.3 Melting of solder interconnects owing to aluminum diffusion

For flip-chip solder joints with an Al/Ni(V)/Cu UBM, if the Ni layer is consumed completely, the adhesion of the UBM to the solder is degraded. In addition, Al diffusion in the Al trace is triggered as a result of the high current density and local heating. Liu and Lin reported an Al flux-induced failure at the cathode side of an Sn97Pb and Sn37Pb composite solder joint with a downward electron flow.[56] Figure 10.8a shows that the location of the Ni layer matched accurately with that of the Cu layer. In the downward electron flow case, the Ni(V) layer would be gradually consumed over a

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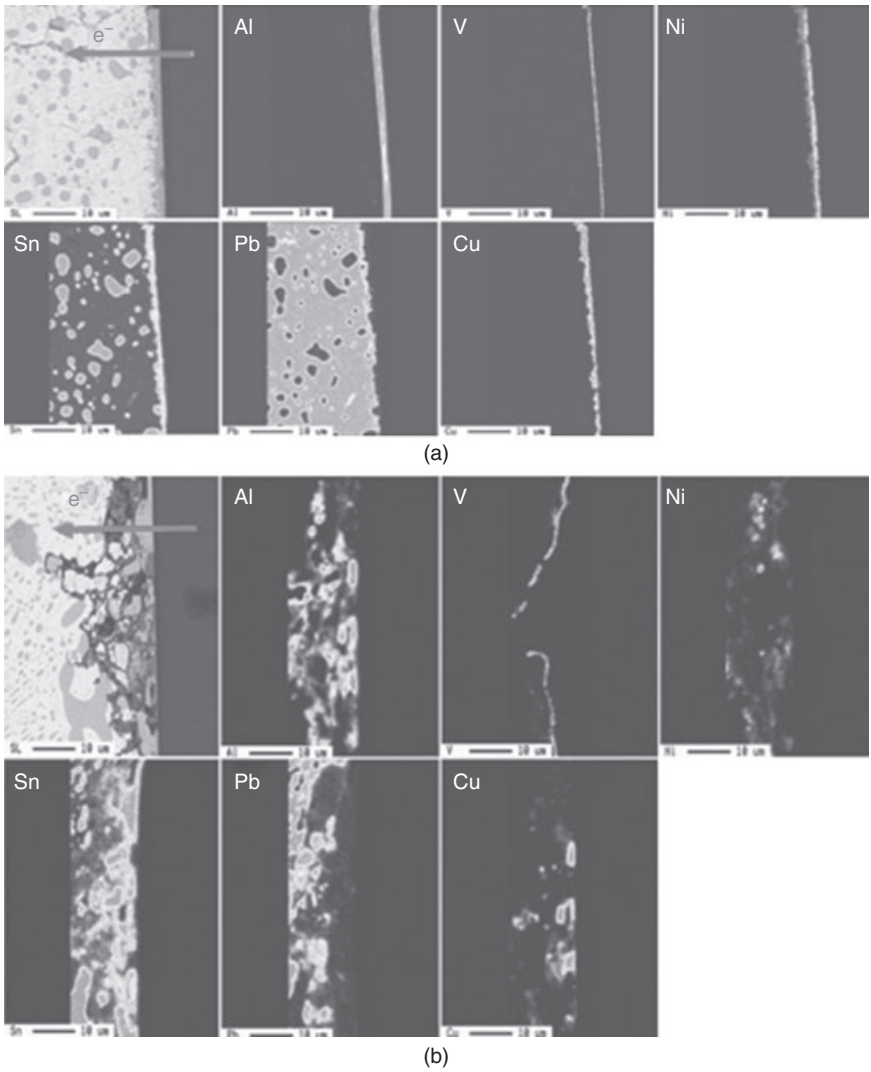


*10.8* Elemental mapping of the interface between a solder and the UBM (a) unfailed after 1000 h current stressing, and (b) failed after 1711 h current stressing.[56]

prolonged period of time. As Fig. 10.8b shows, the Ni completely diffused into the solder and the V layer was also damaged. Furthermore, Al started to spread within the solder joint. EM and the accompanying Joule heating drove the Al away from the Al trace and pushed it into the solder. The diffusion of Al into an Sn3.5Ag solder was also detected by Shao *et al.*[57] They found that the solder filled in where a Ti/Cr-Cu/Cu UBM had been located,

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and $CuAl_2$ IMC formed in the region where the Al pad had been situated.

Using an infrared microscope Liang *et al.* detected the fracture of an Al trace while the current density through the Al trace was about $1.2 \times 10^6$ A cm$^{-2}$.[58] They speculated that EM damage had also occurred in the Al trace, and that the degradation of the Al trace may be responsible for an abrupt temperature rise. Additionally, their thermoelectric simulations supported this. It was the degradation of the Al trace, instead of void formation, that contributed to the formation of a hot spot.

It has been proposed that solder melting under current stressing is a time-dependent phenomenon.[59,60] According to previous research, the principal reason for an incubation time was attributed to the process of void generation and propagation, and solder lifetime was explained through modeling void accumulation.[24,41] However, Ouyang *et al.* have observed the melting of eutectic Sn37Pb solder joints owing to the Joule heating of the Al traces.[59] They suggested that Al dissolution expedited the rise of a solder interconnect's electrical resistance and hence led to the final melting of the solder. Because the resistance change of the Al trace was dependent on the dissolution rate of Al into the solder, an incubation period was required for a temperature rise that could provide sufficient heat to melt the solder joint. In this way, Ouyang *et al.* explained why the melting of the solder exhibited a time-dependent characteristic.

Recently, the melting failure of Sn3.5Ag1.0Cu solder interconnects has been studied under a current density of $2.3 \times 10^4$ A cm$^{-2}$ at 125 °C.[61] A new failure mechanism involving the combined effect of solder EM and Al diffusion has been proposed. Figure 10.9 shows typical stages of the morphological evolution. Firstly, with a downward electron flow, voids occurred at the interface between the Cu–Sn IMC layer and the solder, especially in the current crowding region (Fig. 10.9a). Secondly, as Fig. 10.9b shows, the voids gradually extended to the surrounding areas owing to vacancy supersaturation. Thirdly, the creation of pancake-type voids decreased the effective contact area, which led to more serious current crowding. Meanwhile, the Joule heating owing to current crowding was enhanced because of poor heat dissipation around the voids. Under such accumulated effects, the atomic diffusion of Ni(V) in the UBM was accelerated, and the barrier that prevents the dissolution of Al into the solder no longer existed. Therefore, the diffusion of Al was triggered and some voids were found in the Al pad, as demonstrated in Fig. 10.9c. Also, the local magnified micrograph shown in Fig. 10.9f demonstrates that the Ni(V) layer previously attached to the Al pad had disappeared as compared with Fig. 10.9e. Ni atoms were dissolved and consumed to form a Cu–Ni–Sn ternary IMC, and the V layer above the voids extruded and began to lose its structural integrity, so that the dissolution of Al through this layer was more rapid. Fourthly, with the

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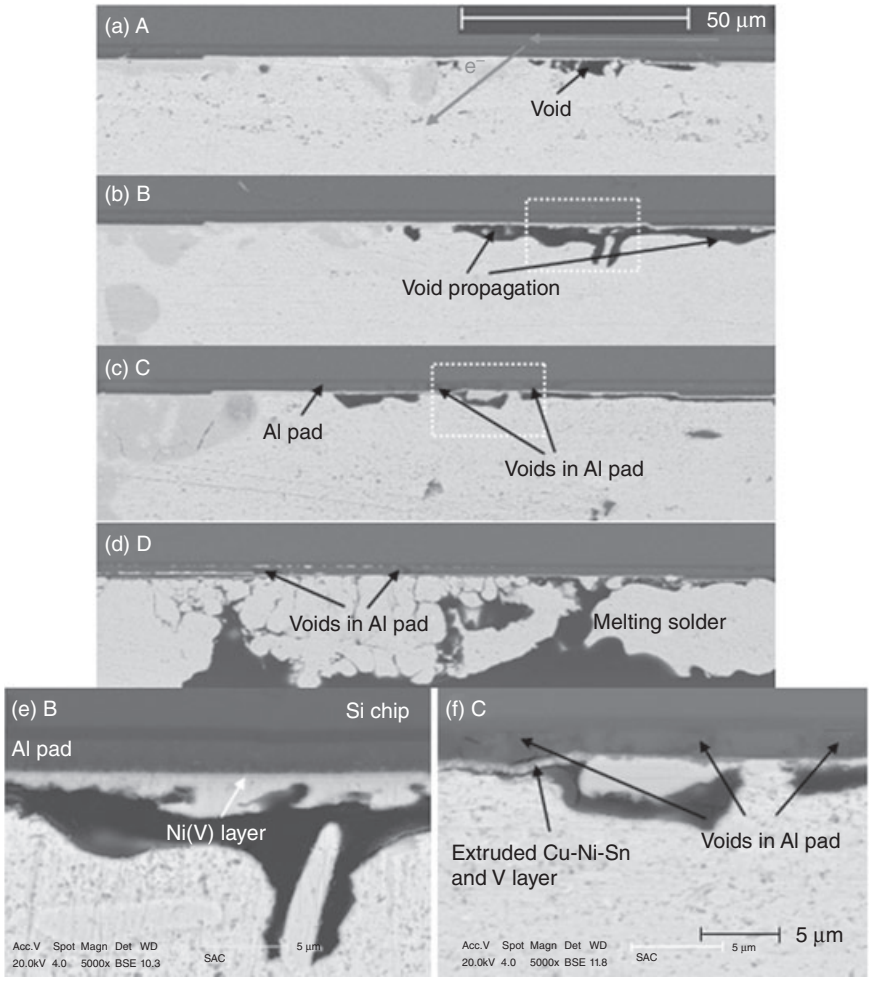


*10.9* SEM images of different stages of the morphological evolution in Sn3.5Ag1.0Cu solder joints under a current density of $2.3 \times 10^4$ A cm$^{-2}$ at 125 °C after (a) 92 h, 25% of the failure time, time point A, (b) 245 h, 66%, B, (c) 295 h, 80%, C, (d) 361 h, 98%, D, (e) local magnified micrograph of the interface at time point B, the dotted region in (b), and (f) C, the dotted region in (c).[61]

progress of Al dissolution, the dramatic Joule heating may damage the interfacial integrity between the Al trace and the passivation layer, as shown in Fig. 10.9d. More significantly, EM in the connecting Al trace was initiated and expedited, so that further melting failure of solder interconnects was produced.

A finite element simulation was applied to understand the current density distribution in the flip-chip interconnects. Figure 10.10 displays the

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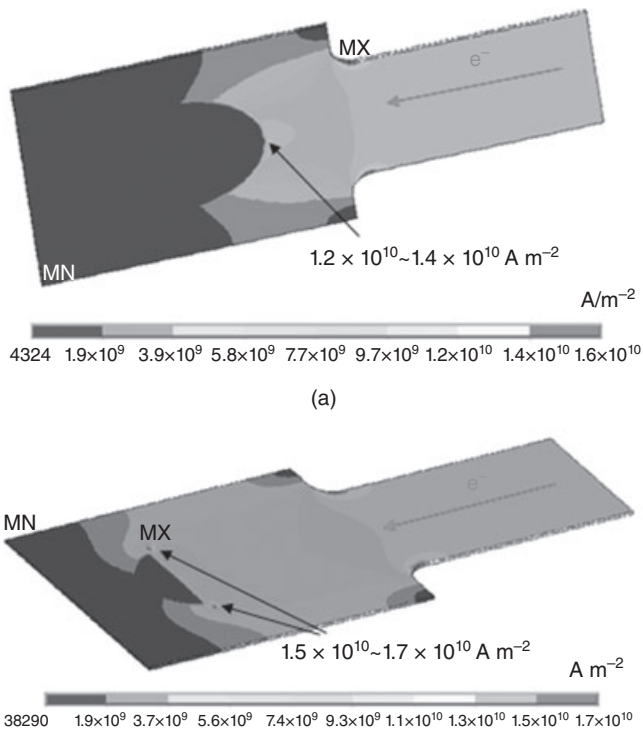
evolution of the current density in Al interconnects alone (as viewed from underneath). The current density reached more than $10^6$ A cm$^{-2}$, which is sufficiently high for triggering the EM of the Al. According to Fig. 10.10a, the current density at the exit location of the Al pad ranged from $1.2 \times 10^{10}$ to $1.4 \times 10^{10}$ A m$^{-2}$ (i.e., from $1.2 \times 10^6$ to $1.4 \times 10^6$ A cm$^{-2}$) before voids were developed. The modeled maximum value occurred at the connecting corner of the Al pad and the Al trace. By contrast, when the voids propagated, the location of the maximum current density was transferred to the exit location of the Al pad, and it reached $1.7 \times 10^{10}$ A m$^{-2}$ (i.e., $1.7 \times 10^6$ A cm$^{-2}$), as shown in Fig. 10.10b. This simulation indicates that the current density through the Al pad was enhanced owing to the decrease of contacting area at the interface, and this result supports the experiments.




*10.10* Current density distribution in the Al interconnect alone (as viewed from underneath): (a) before void growth (current density at the exit location was $1.2 \times 10^{10}$~$1.4 \times 10^{10}$ A m$^{-2}$), and (b) after void growth (current density at the exit location was $1.5 \times 10^{10}$~$1.7 \times 10^{10}$ A m$^{-2}$).[14]

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The total incubation time for melting the solder was dependent on the rates of void growth and Al diffusion in this instance. Therefore, the solder melting exhibited a unique time-dependent characteristic. In the initial stages, the rate of void growth varied from 0.24 to 0.53 μm $h^{-1}$. This rate was related to the void nucleation and propagation. In the later stage, before the final failure, the depletion of the Al also exhibited a linear relationship with time, which was ascribed to the EM of the Al interconnect.

It has been known that the change in trace resistance is a linear function of the atomic drift velocity.[62] In this case, the relationship between the rates of trace resistance change ($\partial(\Delta R/R)/\partial t$) and material depletion ($\partial(\Delta L)/\partial t$) may be described as:

$$\frac{\partial(\Delta R/R)}{\partial t} \approx \left(\frac{\rho_r S_{Al}}{\rho_{Al} S_r} - 1\right)\frac{1}{L}\frac{\partial(\Delta L)}{\partial t} \propto \frac{\partial(\Delta L)}{\partial t} = v_d \qquad [10.4]$$

where the subscripts *r* and Al refer to the under-layer and Al trace, respectively, $\rho$ is the electrical resistivity, $S$ is the cross-sectional area of the specific layer, $R$ is the initial trace resistance, $L$ is the initial trace length, and $v_d$ is the atomic drift velocity. Based on an electrical characteristic, the rate of resistance change was estimated to be 0.9% $h^{-1}$. This rate of change then represents the drift of Al atoms in the later stage.

## 10.4 Stress-related degradation of solder interconnects under EM

### 10.4.1 Morphological evolution owing to EM and a back stress in solder interconnects

When atoms are driven from the cathode to the anode by the electron wind force, the latter are in compression and the former in tension. In a cross-sectioned solder joint for an *in situ* observation, it is expected that the compressive stress is released from the free surface, causing hillocks or whiskers to occur at the anode. Using thin film solder strips, Liu *et al.* first investigated the formation of atomic hillocks in pure tin under a current density of $10^5$ A $cm^{-2}$ at room temperature.[12] An explanation was given in terms of a stress relief mechanism that a hillock or whisker grows from the surface under compression.[63]

Synchrotron X-ray microscopy has been applied to provide information regarding a depth profile for the accumulated stresses.[64,65] Figure 10.11 demonstrates the hillock and valley formation in a eutectic tin–lead solder joint under a current density of $10^4$ A $cm^{-2}$ after 72 h. The depth profile obtained with confocal laser microscopy for the joint, which is shown next to the micrograph, indicates that the maximum height of the hillocks near the anode was about 16 μm, and the depth of the valley near the cathode

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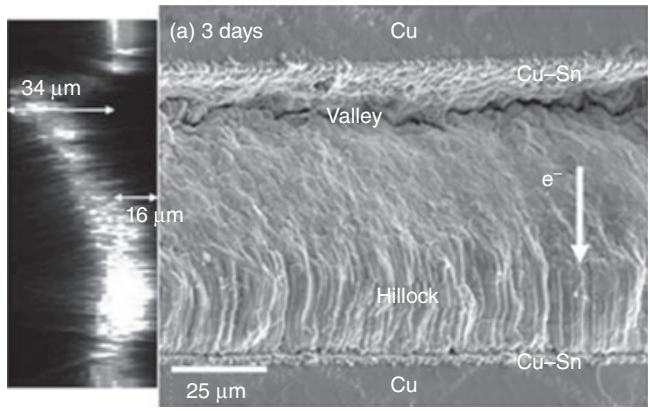


*10.11* Hillock and valley formation in a eutectic tin–lead solder joint under a current density of $10^4$ A $cm^{-2}$ after 72 h (The depth profile is shown to the left).[65]

was about 34 μm. It can also be seen that the surface features of the hillock region exhibited rows of striations with a spacing of several micrometers. These striations were on the side of the hillock facing the anode, and initiated from the anode end then propagated in the direction opposite to the electron flow during current stressing. Such markings can be considered as an indication of the material forced out as a result of the compressive stress.

Ouyang *et al.* reported the formation of whiskers in solder joints.[66] Figure 10.12a and 10.12b show the growth of whiskers at the upper right corner (anode side) in eutectic SnPb and SnAgCu solder joints under a current density of above $10^4$ A $cm^{-2}$ after 48 h and 248.5 h, respectively. The composition of the whiskers was confirmed as 93 wt% Sn by EDX. These whiskers initiated from the cracked surface at the chip side. When Pb atoms were pushed towards the anode, a compressive stress on Sn-rich grains was produced and then Sn whiskers were forced out. Moreover, it was noticed that the cross-sectioned surface of the SnPb solder exhibited a dimple and bulge structure after EM, whereas the surface of SnAgCu solder remained flat. This phenomenon suggests that the rate of EM in SnAgCu was smaller than that in SnPb.

On the basis of the Nabarro–Herring model of the equilibrium vacancy concentration, more vacancies are generated in the tensile region, whereas fewer vacancies occur in the compressive region; therefore, the vacancy concentration gradient decreases from the cathode to the anode.[67] The atomic flux under a combined electrical and mechanical force can be expressed as:

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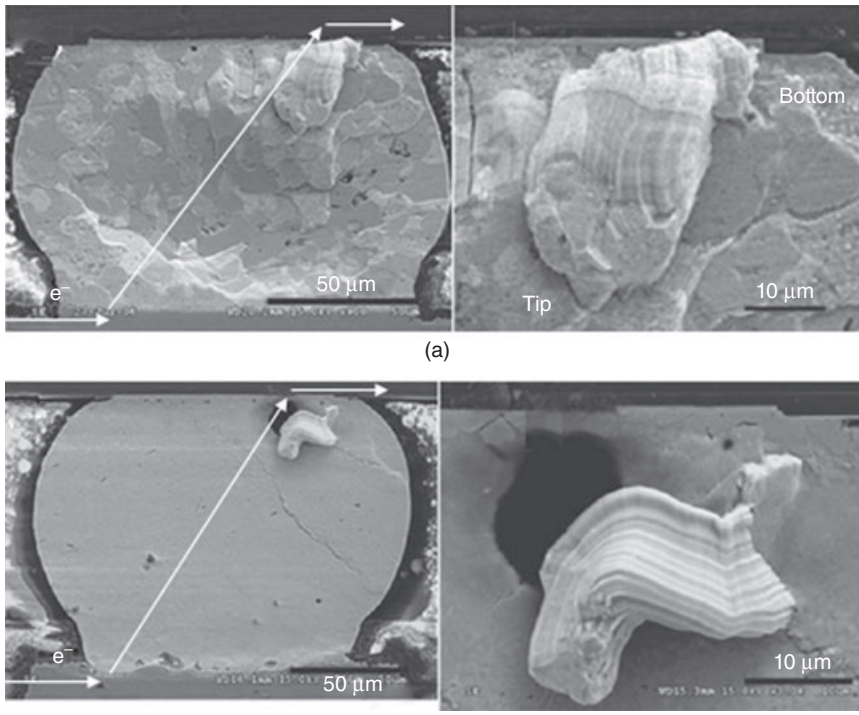


*10.12* Whisker growth at the anode (chip side) (a) a eutectic SnPb solder joint under a current density of $10^4$ A cm$^{-2}$ after 48 h, and (b) SnAgCu solder joint under a current density of $1.4 \times 10^4$ A cm$^{-2}$ after 248.5 h.[66]

$$J = C\frac{D}{kT}Z^*e\rho j - C\frac{D}{kT}\frac{\Omega \mathrm{d}\sigma}{\mathrm{d}x} \qquad [10.5]$$

where $\sigma$ is the hydrostatic stress, $\mathrm{d}\sigma/\mathrm{d}x$ is the stress gradient, and $\Omega$ is the atomic volume. The other terms have been defined before. The first part represents the flux owing to EM, whereas the second part stands for the opposite flux owing to back stress.

A plausible explanation for the above difference between the rates of EM of SnAgCu and SnPb is then given in terms of the back stress.[66] Because the elastic modulus or stiffness of the SnAgCu solder is larger than that of the SnPb, the back stress gradient in SnAgCu could be higher. Hence, the effect of the back stress on the retardation of EM was relatively larger for the SnAgCu solder.

If stress balances with wind force at a critical length, there should be no net atomic flux ($J = 0$), which has been well known as the Blech

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condition.[68] According to equation [10.5], the critical length ($X_c$) can be obtained:

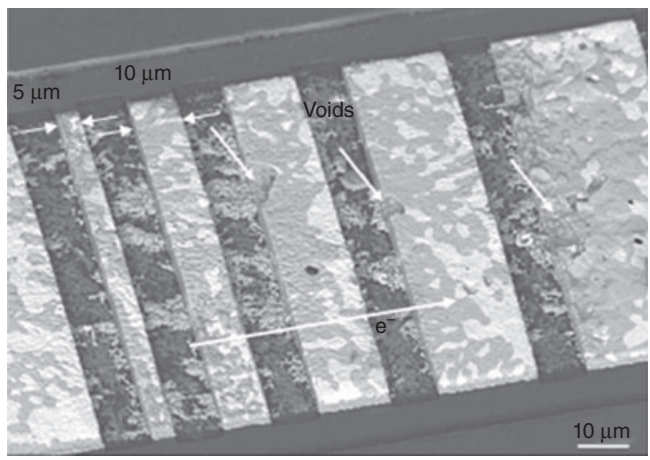
$$X_c = \frac{\sigma_c \Omega}{Z^* e \rho j} \quad [10.6]$$

The effect of back stress and the critical length in a solder was investigated by Wei and Chen.[69] In Wei and Chen's study, eutectic SnPb solder strips with lengths ranging from 5 to 200 μm were prepared and a length-dependent EM behavior was identified. Figure 10.13 shows the microstructural characteristics of various solder strips under a current density of $2 \times 10^4$ A cm$^{-2}$ after 490 h at 100 °C. No material depletion or voids could be detected for the 5 and 10 μm long strips. By taking the critical compressive yield stress ($\sigma_c$) of SnPb solder (27 MPa), the critical length was estimated to be 11 μm under such experimental conditions. This value agrees with the experimental results.

The effect of the back stress was further studied by an area array of nanoindentation markers on the cross-section of solder joints by Xu *et al.*[70] Most markers moved against the EM-induced atomic flux, indicating that in this instance the effect of the electron wind force was larger than that of the back stress. After 360 h of current stressing, the average marker movement from the cathode to the anode was plotted, as shown in Fig. 10.14a.

Also, the atomic flux can be calculated as follows:

$$J = \frac{V}{\Omega(St)} = \frac{u}{\Omega t} \quad [10.7]$$




*10.13* Microstructural characteristics of various solder strips under a current density of $2 \times 10^4$ A cm$^{-2}$ after 490 h at 100 °C (no material depletion could be detected for the 5 and 10 μm long strips).[69]

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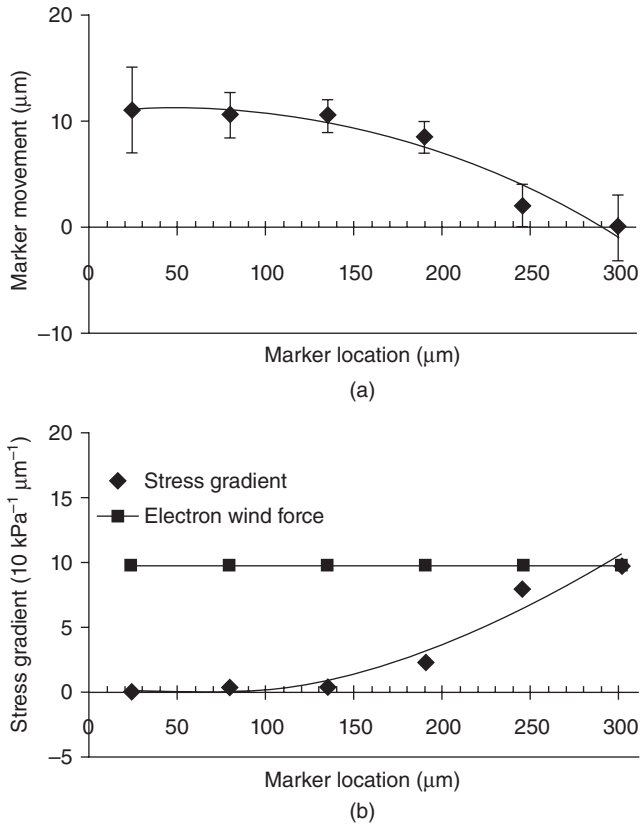


*10.14* (a) Marker movement at different locations in a solder joint under current stressing after 360 h, and (b) the stress gradient as a function of the location.[70]

where $V$ is the total volume of atomic transport, $u$ is the marker displacement, $\Omega$ is the atomic volume, $S$ is the cross-sectional area, and $t$ is the operation time.

By combining equations [10.5] and [10.7], and assuming that the effect of the back stress gradient on the marker movement could be neglected when the marker was far enough from the anode, the stress gradient as a function of the marker displacement. When defining $K = (1/C)(kt/D)(1/\Omega^2 t)$ can be described as:

$$\frac{\mathrm{d}\sigma}{\mathrm{d}x} = K(u_\mathrm{o} - u) \qquad [10.8]$$

where $u_\mathrm{o}$ is the marker displacement near the cathode, and $K$ is a constant for a given temperature and time.

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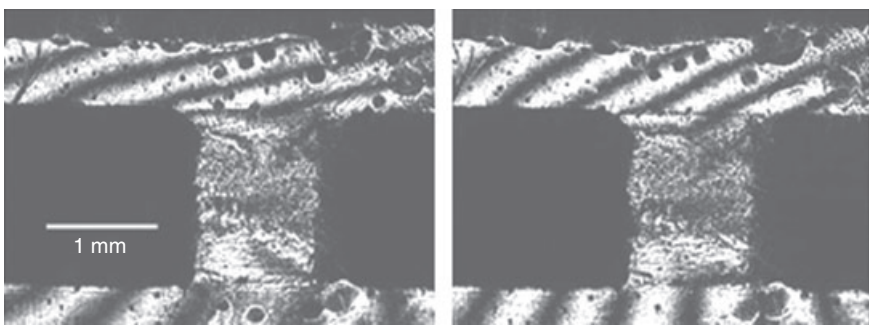
Hence, the stress at any location is:

$$\sigma = \int_0^x K(u_o - u)\mathrm{d}x \qquad [10.9]$$

Substituting $u(x)$ and the boundary conditions into equation [10.9], the stress gradient at any location could be determined, as shown in Fig. 10.14b. The stress gradient near the anode was 97 kPa $\mu m^{-1}$, and it decreased gradually to zero with distance.

## 10.4.2 Mechanical deformation and degradation under current stressing

To detect the EM-induced mechanical damage, a Moiré interferometric technique was used to obtain the *in situ* displacement evolution of solder joints under electric current stressing.[71] Large deformations may be observed in solder joints under a current density of $10^4$ A $cm^{-2}$. Figures 10.15a and 10.16a display the U field and V field fringes in an Sn4Ag0.5Cu solder joint after 1500 h of current stressing, respectively. The U field fringes were predominantly in the vertical direction with concentrations on both vertical edges, indicating that a large normal deformation was developed in the horizontal direction. Instead, the V field fringes were predominantly in the horizontal direction, suggesting a large normal deformation in the vertical direction. In addition, Fig. 10.15b and Fig. 10.16b show the field fringes after the current was switched off. Although the fringes became less clear, there were little changes in both U and V field fringes. This means that the deformations created by the high current density were irreversible, which is attributed to both the re-arrangement of defects and atoms in the material and also the accompanying local volumetric change.




*10.15* U field fringe of an Sn4Ag0.5Cu solder joint (a) during current stressing, and (b) after the current was terminated.[71]

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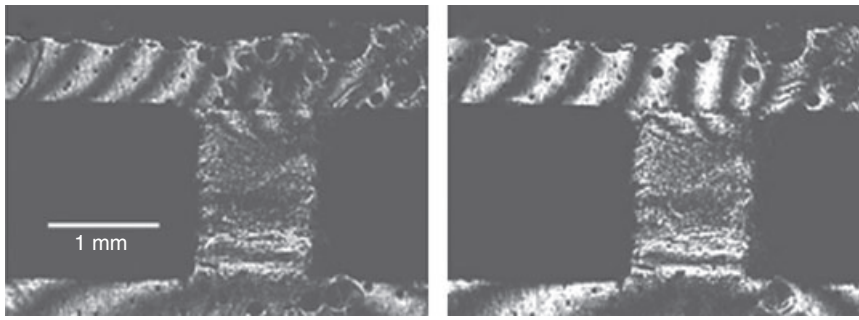
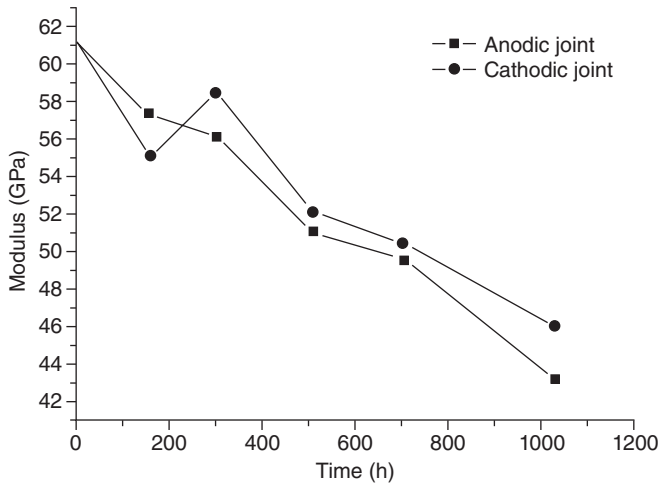



*10.16* V field fringe of an Sn4Ag0.5Cu solder joint (a) during current stressing, and (b) after the current was terminated.[71]




*10.17* Variation of modulus of Sn3.5Ag1.0Cu solder joints under a current density of $2.0 \times 10^4$ A cm$^{-2}$ after various times at 125 °C.[14]

Nano-indentation tests were conducted to explore the mechanical behavior of solder joints after EM.[14] Figure 10.17 illustrates the modulus variation of Sn3.5Ag1.0Cu solder joints under a current density of $2.0 \times 10^4$ A cm$^{-2}$ after various stressing times at 125 °C. It is apparent that the modulus of solder joints decreased after current stressing, and the mechanical properties were degraded compared with the original values. Therefore, when interfacial voids are initiated owing to flux divergence under EM, bond damage occurs in solder joints. From a physical perspective, the modulus is directly related to the atomic bonds. Hence, it is understandable that the modulus decreased with the passage of time under current stressing.

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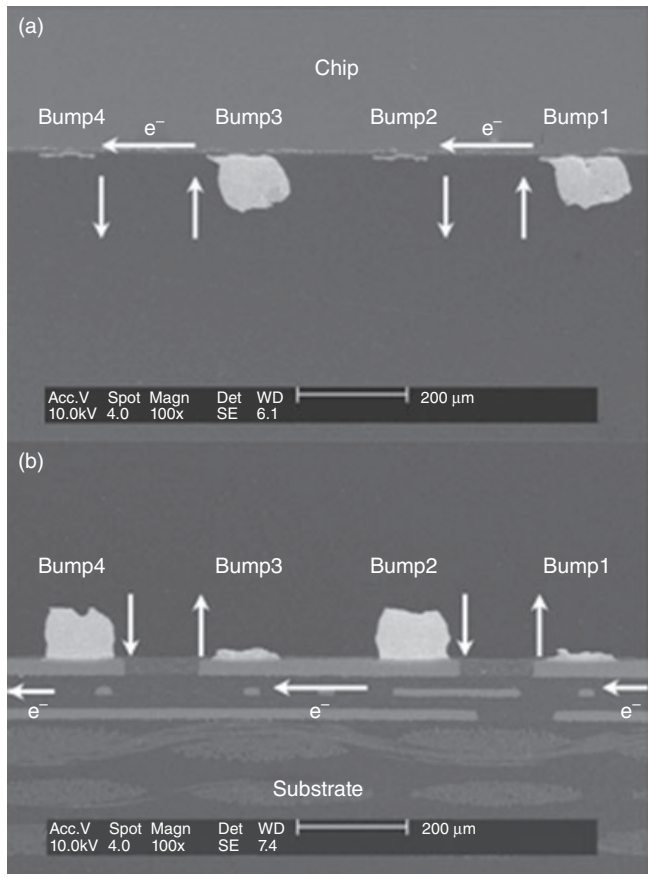
The effect of EM on the shear behavior of flip-chip solder joints was studied by Nah *et al.*[72] It was found that the mode of shear failure changed after EM and depended on the direction of electron flow. Originally, shear-induced fracture occurred in the bulk of the solder without current stressing. However, as shown in Fig. 10.18, under a current density of $2.55 \times 10^4$ A cm$^{-2}$ after 10 h at 140 °C, fracture occurred instead at the cathode interfaces between the solder and IMCs. This is because EM dissolved and drove Cu or Ni atoms from the UBM or bond pad into the solder, resulting in the large growth of brittle Sn-based IMCs at the cathode side. Therefore, shear failure occurred predominantly at the cathode interface.

Also, fractographs of solder joints before and after EM were examined for a comparison.[18] Figure 10.19 shows the typical sheared fracture surfaces




*10.18* SEM images of solder joints after mechanical shear testing under a current density of $2.55 \times 10^4$ A cm$^{-2}$ after 10 h at 140 °C (a) chip side, and (b) substrate side.[72]

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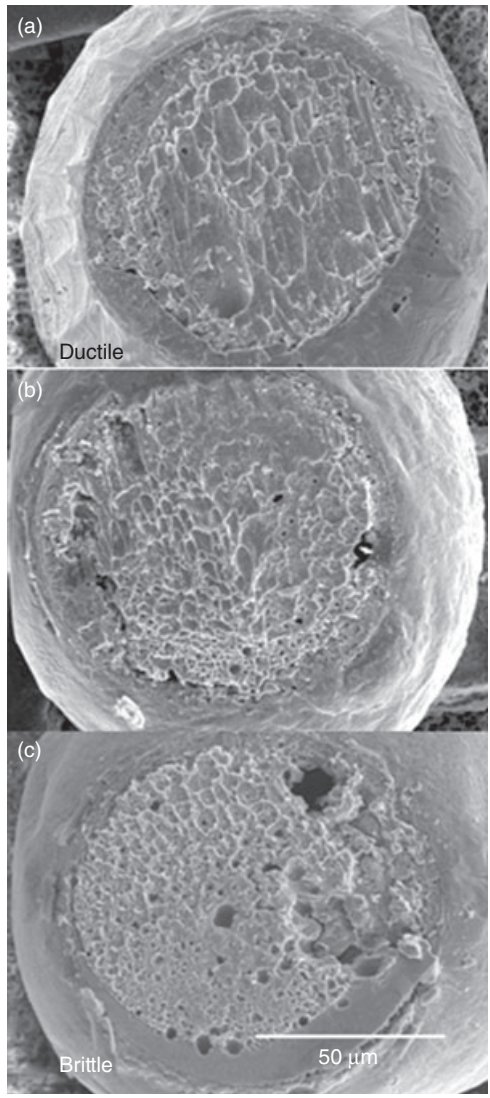


*10.19* Typical fractographs of Sn3.5Ag1.0Cu solder joints (substrate side) (a) as reflowed, (b) under current stressing after 144 h, and (c) under current stressing after 288 h.[18]

of Sn3.5Ag1.0Cu solder joints (substrate side) under a current density of $2.1 \times 10^4$ A cm$^{-2}$ at room temperature. During the test without current stressing, the fracture mode was in the bulk solder cutting through the region just near the $(Cu,Ni)_6Sn_5$ IMC layer, and the fracture surface exhibited great amounts of ductile deformation with large dimples. At longer

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stressing times, the interface became brittle and a smaller amount of plastic deformation was observed. This mechanical deterioration with changes in stressing time is attributed to void formation and stress accumulation at the interface.

## 10.5 Thermomigration (TM) behavior in solder interconnects under a thermal gradient

With the trend towards greater integration and further miniaturization in the microelectronics industry, the cross-sectional area of conductive lines on chips has been decreased significantly. This decrease has led to a dramatic accumulation of Joule heating in first-level interconnects, as discussed in 10.3.1. Then a considerable thermal gradient could build up across solder joints, thus providing a driving force for atomic diffusion to trigger TM.

### 10.5.1 TM in tin–lead solder interconnects

The earliest report regarding the combined effects of EM and TM in solder joints was given by Ye *et al.*[73] With microstructural observations and marker measurements, Ye *et al.* found that TM in flip-chip solder joints may assist or counter EM, depending on the direction of the thermal gradient and electric field.

The individual contribution of TM to the failure of solder joints was described by Huang *et al.*[74] They proposed the design of a test structure of flip-chip solder joints that can be applied to conduct TM without EM. Generally, in the interconnect structure, the Al traces are the primary heat sources because of their large resistance. Hence, it is believed that a certain thermal gradient exists in the powered solder joints as a result of the temperature difference. Moreover, owing to the excellent thermal conductivity of the silicon chip, a similar thermal gradient is also formed across the adjacent unpowered solder joints. These unpowered solder joints are thus investigated for a TM study since no current is applied to them.

Morphological evolution owing to TM has also been detected in eutectic tin–lead solder joints. Figure 10.20a shows SEM images of a row of tin–lead solder joints after 50 h at 150 °C. Figure 10.20b demonstrates the detailed microstructure of joint 4 at a higher magnification.[75] According to these micrographs, it is believed that Pb migrated to the substrate side under the temperature gradient across the unpowered solder joints. This was supported by the EDX analysis of local regions. As shown in Fig. 10.20b, the average concentration of accumulated Pb at the substrate side was about 65.2 at%, and the concentration of Sn at the chip side approached 86.3 at%. The width of the accumulated Pb-rich phase band reached approximately

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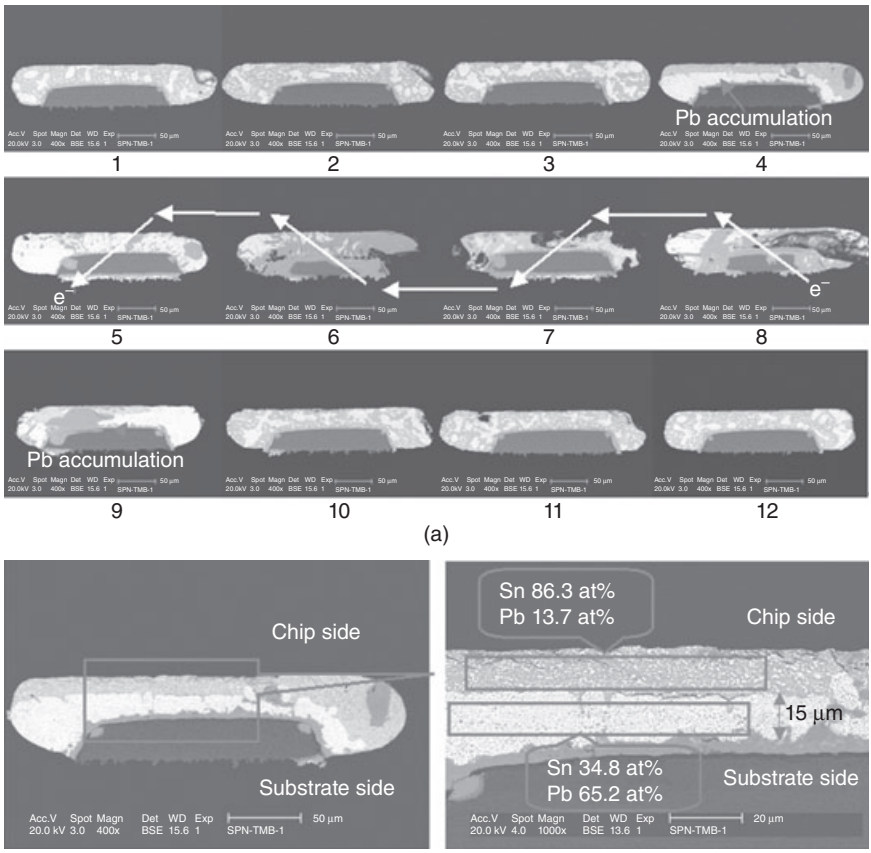


*10.20* (a) SEM images of a row of solder joints from 1 to 12, with solder joints from 5 to 8 under current stressing after 50 h at 150 °C (Pb accumulation in the unpowered solder joints 4 and 9), and (b) the detailed microstructure of joint 4 at a higher magnification.[75]

15 µm, i.e., half of the joint standing height. This result agrees with TM in tin–lead composite flip-chip solder joints.[74]

A possible explanation for the above microstructural evolution is as follows. The flow of atoms under a thermal gradient depends on the heat of transport ($Q^*$), defined as the difference between the heat carried by the moving atoms and the heat of the atoms in the initial state (the hot end or the cold end).[76] For the atoms which move from the hot end to the cold end, the $Q^*$ is negative because they lose heat. For atoms moving from the cold to the hot end, the $Q^*$ is positive. Pb atoms are the dominant diffusing species with a higher diffusivity in eutectic tin–lead solder above 120 °C[77,78] Therefore, based on the microstructural evolution as shown in Fig. 10.20, it

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is speculated that with a negative $Q^*$, Pb atoms migrated from the higher temperature side to the lower temperature side under the temperature gradient. Meanwhile, Sn atoms moved slowly and replenished the vacancies owing to the depletion of Pb atoms. Macroscopically, the Pb-rich phase migrated to one side and the Sn-rich phase was 'pushed' towards the opposite side on the basis of a constant volume process. However, the mechanism of the reversed Sn flux during TM remains unclear, and the sign of $Q^*$ for Sn cannot be confirmed as yet.

It is important to obtain the temperature distribution of first-level solder interconnects to understand the TM behavior of solder joints. Finite-element modeling and simulation were applied to predict the electrothermal characteristics, and the result showed that a temperature gradient greater than 1000 °C $cm^{-1}$ built up across the unpowered joint owing to the Joule heating from the neighboring Al traces.[75] A simulation by Ye *et al.* also showed the existence of a thermal gradient of about 1500 °C $cm^{-1}$ in flip-chip test structures.[73] In combination with the simulation, thermocouples and the temperature coefficient of resistance method were used to verify real temperatures in solder interconnects.[79] However, because of the unique interconnect structure and the limitation of these measurement methods, it is difficult to pinpoint the temperature gradient across solder joints. Recently, a thermal infrared technique was employed by Hsiao and Chen to obtain the thermal gradient directly in cross-sectioned solder joints.[80] As can be seen from Fig. 10.21a, a uniform temperature distribution occurred in the solder bump before current stressing. Then Fig. 10.21b shows the temperature distribution of a solder joint under an alternating current density of $9.2 \times 10^4$ A $cm^{-2}$. Because there is no EM effect under alternating current stressing, and the alternating current produces a similar Joule heating as the direct current does, the alternating current was applied to independently investigate the TM behavior in solder joints. Figure 10.21c shows the temperature profile along the dashed line in Fig. 10.21b, in which the average temperature at the chip side was 16.0 °C higher than that at the substrate side. The thermal gradient was calculated to be approximately 2143 °C $cm^{-1}$. This trial is significant since it verified the existence of a large thermal gradient across real flip-chip solder joints with experimental data.

In addition, from Fig. 10.20b it is noticeable that the Pb-rich phase accumulated at the lower left side, i.e., the lower-temperature region of solder joint 4. Likewise, the Pb redistribution in solder joint 9 showed a similar tendency, i.e., Pb migrated to the lower right side (the lower temperature region), as Fig. 10.20a shows. As an example, because the right side of solder joint 4 was closer to the heat source, it is possible that a temperature gradient was established laterally from the right side to the left side. Thus the Pb-rich phase not only migrated to the substrate side under the vertical temperature gradient, but also moved to the lower temperature region

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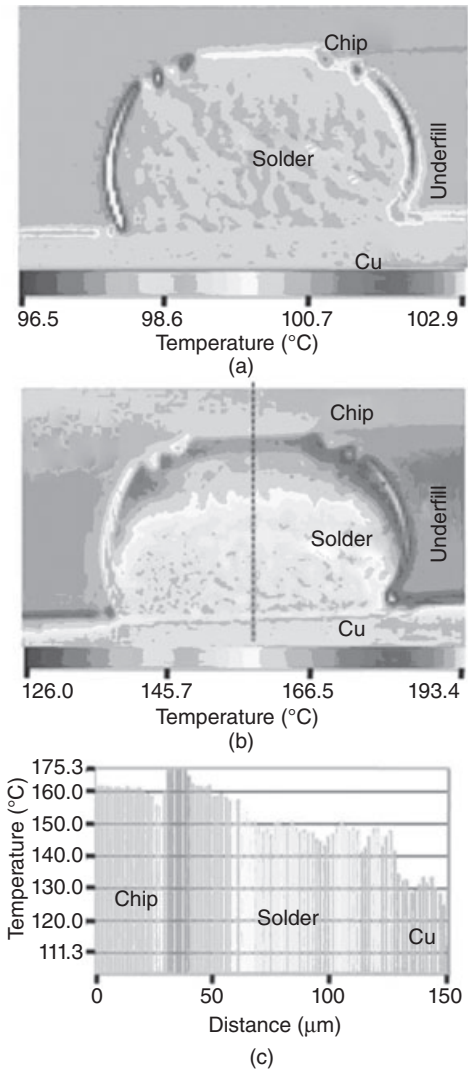


*10.21* (a) Temperature distribution of a solder joint before current stressing, (b) under an alternating current density of $9.2 \times 10^4$ A cm$^{-2}$, and (c) the temperature profile along the dashed line in (b) (the thermal gradient was estimated to be 2143 °C cm$^{-1}$).[80]

driven by the lateral temperature gradient across this solder joint. This lateral TM was also observed in composite solder joints.[74,81]

Morphological variations at different cross-sectional planes of a solder joint during TM are involved because of differing thermal dissipations.[79] Figure 10.22a shows the obvious TM of Pb at the periphery of two solder

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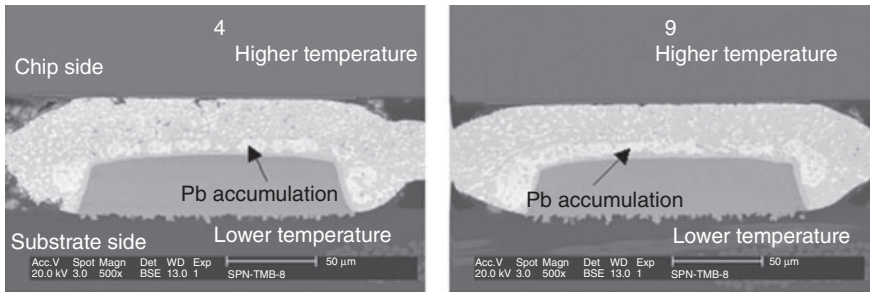
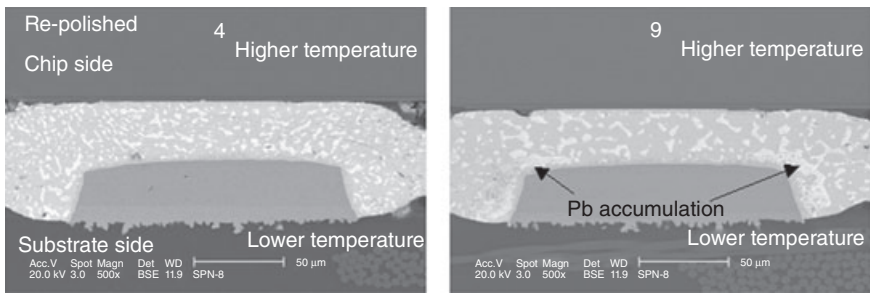



(a)




(b)

*10.22* SEM images of two cross-sectional planes for unpowered solder joints 4 and 9 (a) after the first polishing (outer solder), and (b) after repolishing approximately 50 μm (inner solder).[79]

joints, which is similar to that of Fig. 10.20. Then a stepwise cross-sectional analysis was conducted by gradually grinding the solder joints to the center of the passivation opening. Figure 10.22b demonstrates the cross-sections of solder joints 4 and 9 after re-polishing approximately 50 μm. It is noted that the TM of Pb was not as apparent as that in Fig. 22a. Pb-rich phases were uniformly distributed in solder joint 4. Pb accumulation in solder joint 9 was also slight and only the Pb-rich phase at the periphery of the solder exhibited a TM characteristic. Therefore, the TM of the inner solder region was less significant than that of the outer solder (the surface layer). One can understand that the temperature distribution inside the center of a solder joint became more uniform. By contrast, it is easier for a large thermal gradient to build up across the surface layer of solder joints where a substantial heat dissipation is achieved, because the outer solder is close to the ambient environment.

It is worth mentioning that during the TM, the Pb grains were even more uniformly dispersed in the tin matrix, although the bulk of the Pb had moved to the substrate side, as shown in Fig. 10.20b. This means that the lamellar microstructure became much finer after the TM process. This microstructure change has also been detected in Sn58Bi solder joints under a TM-enhanced

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effect in our group.[82] Ouyang *et al.* found a similar phenomenon.[83] They suggested that the formation of this finer lamellar structure created a more disordered higher entropy state.[2,83] Also, according to their estimate, entropy production by heat propagation was many orders of magnitude larger than that by atomic migration, and it is thus conceivable that entropy production in TM could affect the microstructure substantially.

In order to understand the mechanism of atomic transport, the atomic flux and the heat of transport during the TM process were estimated. Taking a central displacement ($\Delta x$) of 7.5 μm in Fig. 10.20b, the total volume of atomic transport ($V_{tm}$) during the operation time ($t$) can be approximately obtained from the product of the displacement and the cross-sectional area ($S$) of the solder joint. Therefore, taking the atomic volume of Pb ($\Omega$) as $3.0 \times 10^{-23}$ cm$^3$, the atomic flux of Pb owing to TM ($J_{tm}$) can be calculated as follows:

$$J_{tm} = \frac{V_{tm}}{\Omega(St)} = \frac{A\Delta x}{\Omega(St)} = \frac{7.5 \times 10^{-4}}{3.0 \times 10^{-23} \times 50 \times 3600} \approx 1.4 \times 10^{14} (\text{atoms cm}^{-2}\text{s}^{-1}) \quad [10.10]$$

In addition, the atomic flux owing to TM can be expressed as equation [10.2] as shown in 10.1.2. Hence, taking a predicted temperature gradient of 1100 °C cm$^{-1}$, an atomic diffusivity of Pb of $4.0 \times 10^{-13}$ cm$^2$ s$^{-1}$,[78] we substituted these values into equation [10.2], and obtained the molar heat of transport as approximately –27.2 kJ mol$^{-1}$. Compared with the result reported by Ouyang *et al.* (–25.3 kJ mol$^{-1}$),[83] the molar heat of transport of Pb is slightly different.

In addition, Chuang and Liu estimated the molar heat of transport of Pb as –22.2 kJ mol$^{-1}$ under a thermal gradient of 1010 °C cm$^{-1}$, by measuring the displacement of artificial markers.[84] Significantly, they found that the average displacement of atoms increased almost linearly with time during TM. More recently, markers fabricated by a focused ion beam (FIB) method were used to measure the rate of TM by Hsiao and Chen.[80] With a thermal gradient of 2143 °C cm$^{-1}$, a molar heat of transport of –26.8 kJ mol$^{-1}$ has been obtained for the transport of Pb.

## 10.5.2 TM in tin-based lead-free solder interconnects

As stated above, the migration of the Sn flux during TM is unclear and this has necessitated further investigations for lead-free solders. A more recent study by Hsiao and Chen further reveals the TM characteristic of Sn in lead-free solder.[85] They investigated the TM behavior of Sn in Sn3.5Ag solder joints under a temperature gradient of 2829 °C cm$^{-1}$ at 100 °C. As mentioned in 10.5.1, an alternating current was used to eliminate the EM effect, thus facilitating an independent study of TM. After 800 h of TM

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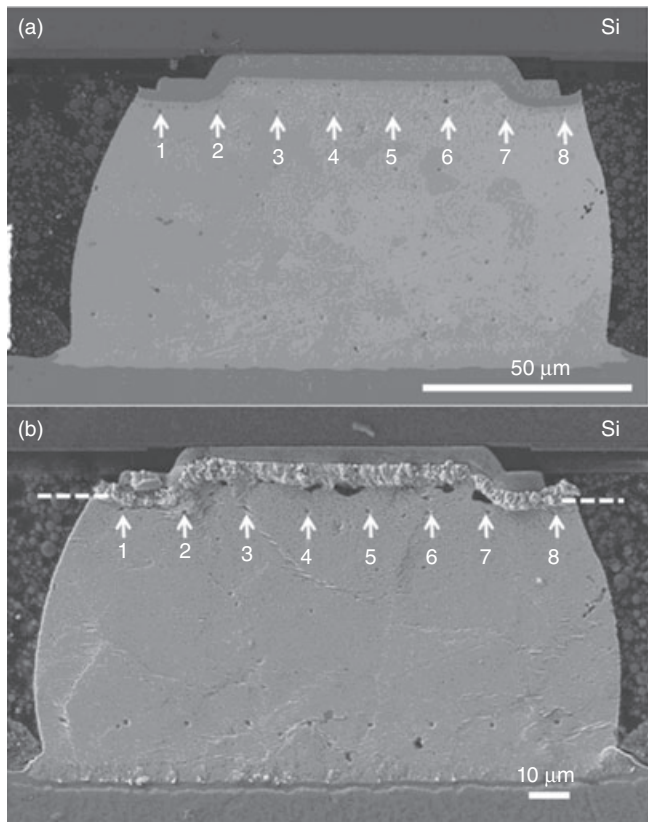
testing with a 0.57 A alternating current, it is significant that hillocks were pushed out from the chip side, as shown in Fig. 10.23b. These hillocks were generated by the mass transfer of the Sn at the hot side, providing direct evidence that Sn was transported along the direction opposite to the thermal gradient. In addition, by measuring the marker movement, they obtained the TM flux and molar heat of transport of Sn as $5.0 \times 10^{12}$ atoms $cm^{-2}$ $s^{-1}$ and 1.36 kJ $mol^{-1}$, respectively, which are smaller than those of Pb atoms listed in 10.5.1. Our studies also show the similar tendency of Sn atoms migrating towards the higher temperature side in Sn3.0Ag0.5Cu solder joints under a thermal gradient.[14,86]

Microstructural evolution in Cu/Sn4Ag0.5Cu/Cu solder interconnects has been studied under a thermal gradient of 1000~1200 °C $cm^{-1}$, and a TM




*10.23* (a) Original micrograph of a Sn3.5Ag solder joint and (b) micrograph of a solder joint after 800 h of TM testing with a temperature gradient of 2829 °C $cm^{-1}$ at 100 °C. (Note that the Sn whiskers were present at the chip side, and the markers moved toward the substrate side.)[85]

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of Cu atoms has been proposed.[87,88] It has been found that the two major microstructural differences between TM and isothermal samples were the lack of a $Cu_3Sn$ layer at both the higher and lower temperature sides, and the thinning of the $Cu_6Sn_5$ layer at the higher temperature side for the TM samples. Supposedly, this thinning of the $Cu_6Sn_5$ layer occurred because of its disintegration, during which the Cu atoms moved to the lower temperature side under the thermal gradient. Meanwhile, the absence of the $Cu_3Sn$ layer was a result of an insufficient Cu concentration. More recently, the TM of interstitial Cu in SnAg flip-chip solder joints was reported by Chen *et al.*[89] Chen *et al.* suggested that the void formation at the chip side was attributed to a fast interstitial diffusion of Cu atoms from the UBM into the Sn matrix. The driving force of Cu diffusion was the result of a large thermal gradient accredited to Joule heating across the solder bumps. Further attempts need to be made to verify the real characteristic of the TM of Cu.

More than that, a specific line-type test structure (Ni/Sn58Bi/Cu) has been applied to investigate the combined effect of EM and TM of Bi, as shown in Fig. 10.24a.[82] As Ni shows a higher electrical resistivity than Cu, a large temperature difference may be created at two sides of the solder joint during the current stressing (downward from the Ni to the Cu side). Finite-element simulation has shown that a thermal gradient of about 527 °C $cm^{-1}$ existed in the solder joint under a current density of $5 \times 10^3$ A $cm^{-2}$ at 50 °C, as demonstrated by Fig. 10.24b and 10.24c. Temperature measurements using thermocouples also supported this thermal gradient. By varying the direction of the electrical current, the counteracted and enhanced effects of TM were detected separately. It can be seen from Fig. 10.25 that the migration of Bi atoms was more pronounced when the Ni wire was used as the cathode. According to the experimental findings, we speculate that the Bi has a similar TM characteristic to Pb and shows a negative $Q^*$. Then, if the direction of the thermal gradient was opposite to that of the electron flow, the TM counteracted the EM and retarded the diffusion of the Bi atoms (case 1). Otherwise, the TM assisted the EM, and the diffusion of the Bi atoms was enhanced (case 2). In addition, based on the results from these two cases, the atomic fluxes of Bi owing to EM and TM were differentiated and estimated to be $1.48 \times 10^{13}$ atoms $cm^{-2}$ $s^{-1}$ and $5.38 \times 10^{12}$ atoms $cm^{-2}$ $s^{-1}$, respectively.

## 10.6 Conclusions

### 10.6.1 Summary

In this review, we have discussed four types of physical failure mechanisms of solder interconnects for high current density applications. Interfacial void

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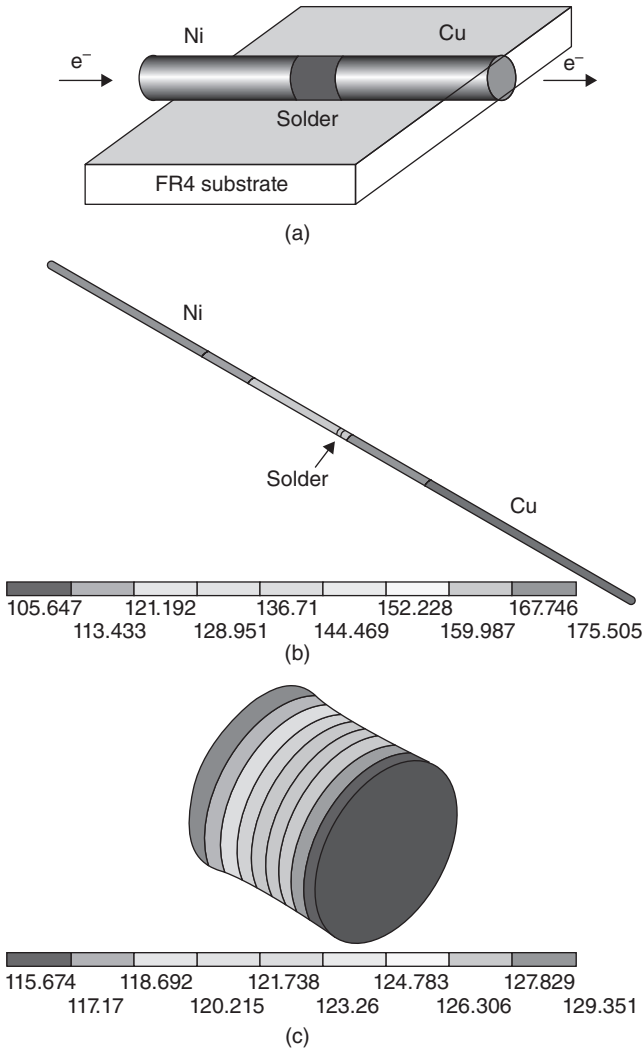


*10.24* (a) Schematic diagram of a line-type test structure (Ni/Sn58Bi/Cu), (b) temperature distribution in the test structure, and (c) temperature distribution in the solder joint only (a thermal gradient of about 527 °C $cm^{-1}$ existed across the solder joint).[82]

growth, the essential physical process occurring in EM, was introduced in 10.2. EM reliability parameters for Sn-based lead-free solder interconnects in recent publications were also collected for summary. The modification of Black's model, which greatly affects the lifetime statistics and reliability evaluation for EM failure, is significant.

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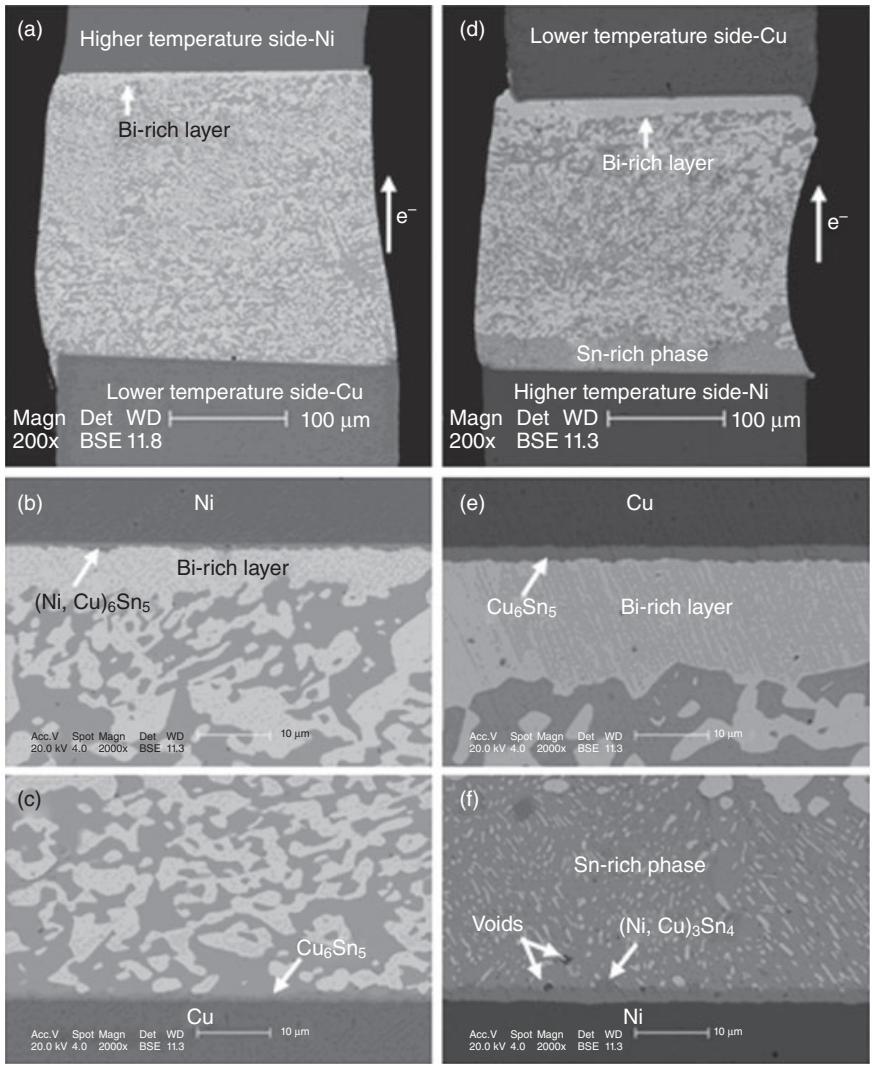


*10.25* SEM images of Ni/Sn58Bi/Cu solder joints under a current density of $5 \times 10^3$ A cm$^{-2}$ after 384 h at 50 °C (a) case 1: EM counteracted by TM, (b) anode side in case 1, (c) cathode side in case 1, (d) case 2: EM enhanced by TM, (e) anode side in case 2, and (f) cathode side in case 2.[82]

Joule heating in first-level solder interconnects is substantial. This was demonstrated in 10.3 through experimental and numerical investigations. Owing to interstitial diffusion enhanced by Joule heating, the consumption of the UBM layer is noticeable so that new structural design (e.g., Cu/Ni pillar) and microstructural improvement need to be developed to support

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high current densities and to minimize EM. In addition, the Al diffusion-induced damage in flip-chip interconnects has attracted some interest in current research. We have proposed a failure mechanism involving the combined effect of solder EM and Al diffusion, and thus offered an explanation for the time-dependent behavior of solder melting failure under current stressing.

We reviewed the stress-related degradation of solder interconnects under a current density in 10.4. Owing to the relief of compressive stresses, morphological evolution is apparent in the form of hillocks or whiskers near the anode. One important factor, the back stress generated, was investigated to understand the damage caused by EM. In addition, the mechanical deformation was identified through an interferometric technique. In addition, the deterioration of solder interconnects under current stressing was detected through a series of mechanical tests.

An attempt to explore the TM behavior of solder interconnects has been made recently, and this was discussed in 10.5. By employing a testing method of differentiating TM from EM, the TM behavior of Pb was understood in terms of morphological evolution, atomic transport and by numerical simulation. Pb shows a negative heat of transport. The TM of Sn has also been studied. On the basis of experimental findings it is speculated that Sn atoms exhibit a different TM characteristic opposite to that of Pb atoms. More recently, the TM of interstitial Cu has been reported, which states that the Cu also has a negative heat of transport. In addition, a specific line-type test structure has been utilized to investigate the combined effect of EM and TM of Bi. It was revealed that Bi has a similar TM behavior to that of Pb.

### 10.6.2 Future trends

The current carrying capability of Al/UBM/solder should be considered based on the limitation owing to EM in the design rules. Routing design of Al interconnects needs to be implemented to mitigate the current crowding and Joule heating. A pad structure that produces a uniform current distribution within the bump interconnect is recommended to avoid the dissolution of Al. In occurrences of EM problems with Al, a relative enlargement of the cross-section of the Al trace is also a factor that could be considered. For UBM, in 10.3.2, the solution of a thick Cu pillar with a Ni electroplated layer has been suggested, which can be expected to alleviate the effect of current crowding and of accompanying heat accumulation at the interface. Our research suggests that new solder technologies with improved current density capabilities and a higher operating temperature will be developed in the near future. Considering the Sn-grain rotation under current stressing, a further nano-doping into solder is anticipated to stabilize the microstructure for limiting the fast interstitial diffusion of noble or near-noble

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metals. In addition, taking into account different applications in industry, EM studies in Sn-based solders should be extended to other lead-free solders, such as InAu.

Although void formation at the UBM side has been confirmed as a major failure mechanism in solder interconnects for high current density applications, IMC growth at the interface cannot be ignored. The extensive IMC growth at the substrate side exerts a great influence on the mechanical reliability. The kinetics dominating interfacial reactions have not yet been established, and the laws of IMC growth (parabolic or linear) under current stressing are still under investigation. Therefore, the interfacial reactions under current stressing are important and challenging problems, particularly for the application of micro-bumps with Cu pillars in 3D packages, such as through silicon via (TSV) bonding, where the IMCs substantially form at the interface; hence, a major phase transformation is induced.[90,91]

Another issue of key importance is the TM of Sn. Although a small number of recent studies exist, the present understanding of the TM behavior of Sn is still limited. To differentiate TM from EM further, it is suggested that each end of the connecting wires (same materials) in a line-type test structure should be set at different temperatures.[92] In this way, the effect of current stressing is completely removed and only the driving force owing to TM is available. As compared with flip-chip samples, the advantages of line-type samples are that the temperature gradient can be measured more easily.

So far, few studies on the combined effect of TM and mechanical stress have been reported.[93] For the mechanical characteristics, high strain rate fracture failure is as important as low cycle fatigue failure, which has been of major concern in recent years. Shear tests and tensile tests should be performed to evaluate the mechanical behavior of solder joints after TM. If atoms migrate from the higher to the lower temperature side by the force caused by the thermal gradient, a reversed flux of vacancies moves to the higher temperature side. Consequently, the interface at the higher temperature side becomes mechanically degraded. Therefore, this interaction between TM and the applied stress is of considerable importance.

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